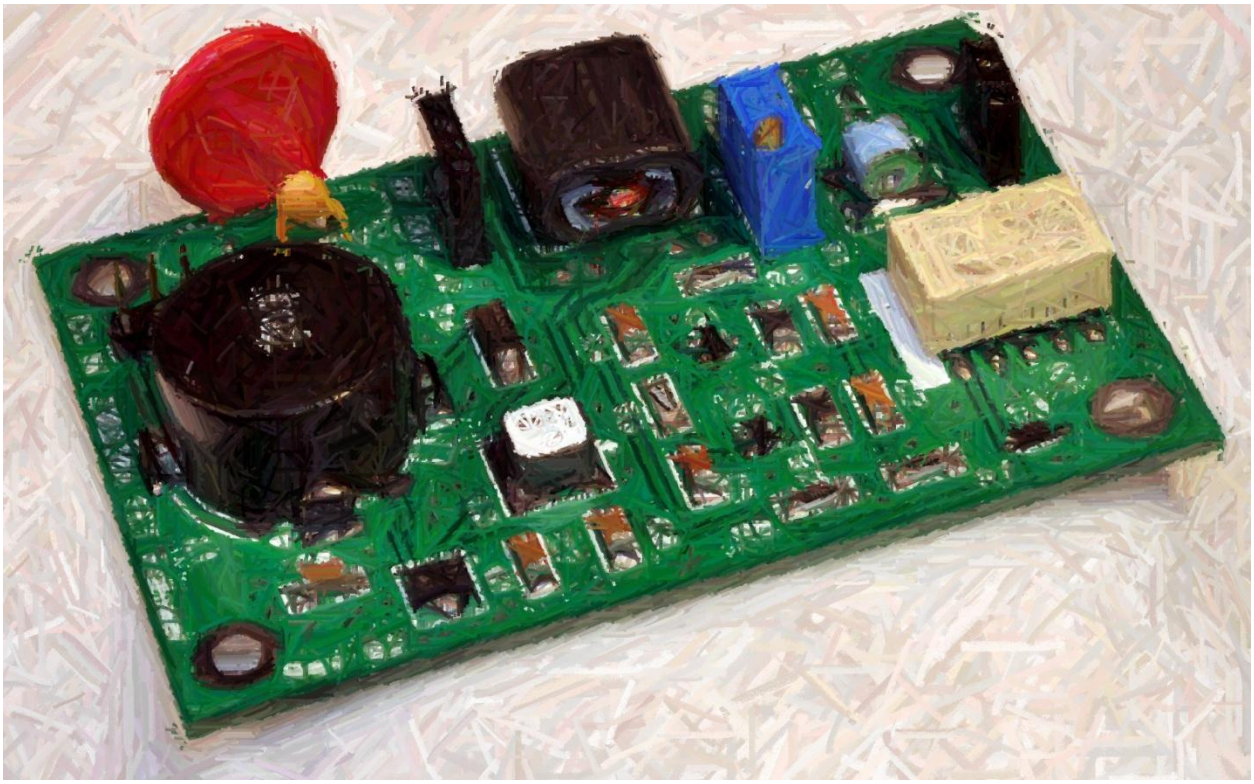
Z10130A FET Follower Amplifier

Construction and Operating Manual



Clifton Laboratories
7236 Clifton Road
Clifton VA 20124-1802
www.cliftonlaboratories.com
(703) 830 0368

Model Z10130A High Gain Amplifier

Revised 15 March 2012

(c) 2012 Jack R. Smith d/b/a/ Clifton Laboratories.

Trademarks and Copyright

Material in this document copyrighted © 2012 Clifton Laboratories. All rights reserved. It is provided to allow the Z10130A purchasers to maintain their equipment and such other purposes as may not be prohibited by law.

Warranty

This warranty is effective as of the date of first consumer purchase.

What is covered: During the ninety (90) days after date of purchase, Clifton Laboratories will correct any defects in the Z10130A due to defective parts (kit or assembled) or workmanship (if purchased as an assembled unit) free of charge (post-paid). You must send the unit at your expense to Clifton Laboratories, but we will pay return shipping. Clifton Laboratories' warranty does not extend to defects caused by your incorrect assembly or use of unauthorized parts or materials or construction practices.

What is not covered: If the Z10130A is purchased as a kit, this warranty does not cover correction of assembly errors or misalignment; repair of damage caused by misuse, negligence, or builder modifications; or any performance malfunctions involving non-Clifton Laboratories accessory equipment. *The use of acid-core solder, water-soluble flux solder, or any corrosive or conductive flux or solvent will void this warranty in its entirety.* Whether purchased as an assembled unit or as a kit, also not covered is reimbursement for loss of use, inconvenience, customer assembly or alignment time, or cost of unauthorized service. Damage due to operating the Z10130A near a transmitting antenna is not covered under the warranty.

Limitation of incidental or consequential damages: This warranty does not extend to non-Clifton Laboratories equipment or components used in conjunction with our products. *Any such repair or replacement is the responsibility of the customer. Clifton Laboratories will not be liable for any special, indirect, incidental or consequential damages, including but not limited to any loss of business or profits.*

Under no circumstances is Clifton Laboratories liable for damage to your equipment connected to the Z10130A resulting from use of the Z10130A, whether in accordance with the instructions in this Manual or otherwise.

Table of Contents

Model Z10130A High Gain Amplifier 1

Trademarks and Copyright 1

Warranty 1

Specifications 3

Overview 3

Assembly 4

Board Outline 4

Recommended Assembly Order 5

Post Assembly Check and Adjustment 9

Adjusting Bias Potentiometer, R1 10

Laboratory Method 11

Off the Air Method 14

Theory of Operation 15

Connections and Operation 16

Troubleshooting 17

Parts List 22

Specifications

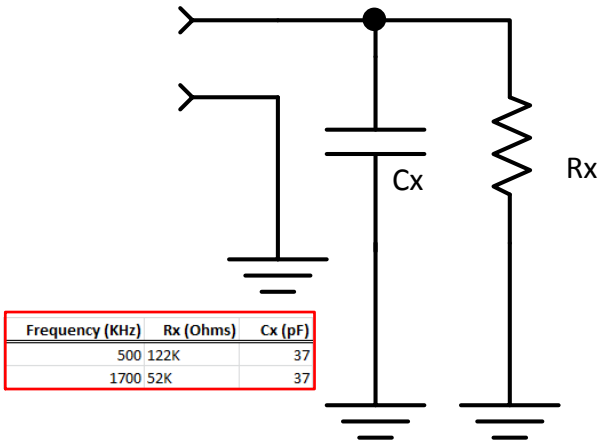
Plots in this Manual are taken from production units but demonstrate typical, not warranted, performance. Clifton Laboratories offers an optional measured performance data for any Z10043A amplifier. Contact Clifton Laboratories for price and availability of measured data.

Overview

The Z10130A is Clifton Laboratories' implementation, with his consent, of the complementary symmetry FET follower designed by Dr. Dallas Lankford and described in his publication "Complementary J310 – J271 FET Follower, 8/21/2011, rev 2/5/2012"

Parameter	Value
Dimensions	The Z10130A printed circuit board is 3.00 inches x 2.00 inches (76.2mm x 50.8mm). Recommend minimum enclosure height is 1.0 inches (25.4 mm). Recommended enclosure Hammond 1590WBFL.
DC Supply	The Z10130A has an on-board 12V low dropout regulator. The DC supply should be in the range of 12.6V to 28V DC at approximately 20 mA. Upon request the Z10130A can be supplied with an on-board 10V low dropout regulator that extends the low voltage limit to approximately 10.8V. There will be some degradation in intermodulation performance with this option.
Gain	Approximately -4 dB into 100 ohm termination at 1 MHz
Frequency Range	-3 dB points with respect to gain at 1 MHz are 50 KHz to > 300 MHz
Intermodulation	Measured with 611 and 703 KHz test tones at 0 dBm per tone, typical input intercepts are: IIP2 +87 to +93 dBm; IIP3 +40 dBm to +45 dBm.
Input Impedance	See Z10130A Equivalent Input Circuit below

Z10130A Equivalent Input Circuit



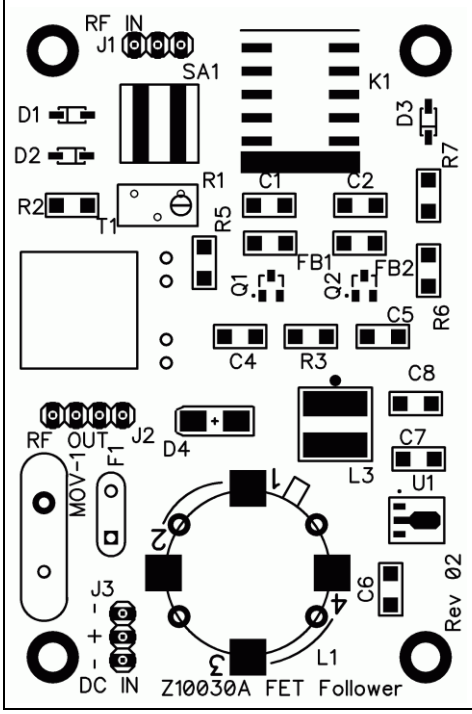
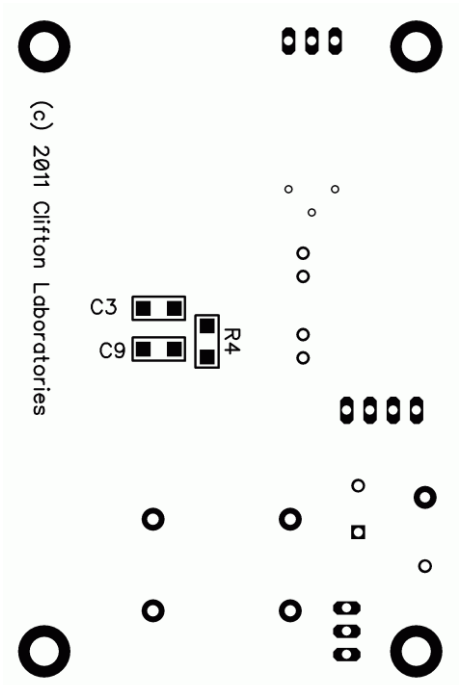
Frequency (KHz)	Rx (Ohms)	Cx (pF)
500	122K	37
1700	52K	37

Assembly

A parts list is provided later in this document. Before assembling the Z10130A you may wish to check the parts supplied against the parts list. This kit assumes you are familiar with surface mount assembly and proper anti-static procedures.

Board Outline

Although the Z10130A printed circuit board is silk-screened with parts identifiers, it can be useful to have an image of the parts location.

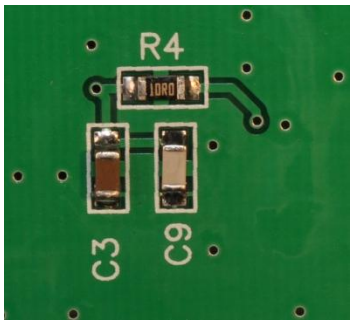
Top Board Surface	Bottom Board Surface
	

Recommended Assembly Order

Bottom PCB Surface

- ❑ Install R4, a 10 ohm resistor, marked 10R0.
- ❑ Install C9, a 100p capacitor, unmarked
- ❑ Install C3, a 1u0 capacitor, unmarked.

This completes the bottom surface installation. Your board should look like the photo at the right.

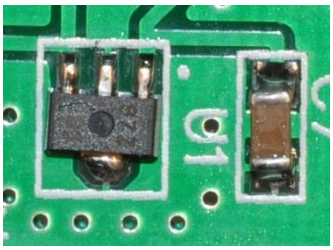


Top PCB Surface

The strategy is to install smaller components first, and larger components last, with some deviation from this strategy to allow for soldering iron clearance.

- ❑ Install R2, a 1M resistor. This may be supplied as a 5% tolerance part, marked “105” or a 1% tolerance part, marked “1004.”
- ❑ Install R5, a 1M resistor. This may be supplied as a 5% tolerance part, marked “105” or a 1% tolerance part, marked “1004.”
- ❑ Install R6, a 1M resistor. This may be supplied as a 5% tolerance part, marked “105” or a 1% tolerance part, marked “1004.”
- ❑ Install R7, an 820K resistor. This may be supplied as a 5% tolerance part, marked “824” or a 1% tolerance part, marked “8203.”
- ❑ Install R3, a 200R resistor. This is a 1% tolerance part, marked “2000.”
- ❑ Install C4, a 1u capacitor, unmarked.
- ❑ Install C5, a 1u capacitor, unmarked.
- ❑ Install C7, a 1u capacitor, unmarked.
- ❑ Install C8, a 1u capacitor, unmarked.
- ❑ Install C1, a 0u1 capacitor, unmarked.
- ❑ Install C2, a 0u1 capacitor, unmarked.
- ❑ Install U1, an MCP1804 12V SOT89 low dropout regulator, marking 87Z. (Additional characters on U1 are for production lot tracing.)

U1’s orientation follows the pad layout, as illustrated.



- ❑ Install C8, a 1u capacitor, unmarked.
- ❑ Install FB1, a ferrite bead, unmarked.

❑ Install FB2, a ferrite bead, unmarked.

Q1 and Q2 are installed next. Both are junction FET devices and normal anti-static precautions should be followed during their installation.

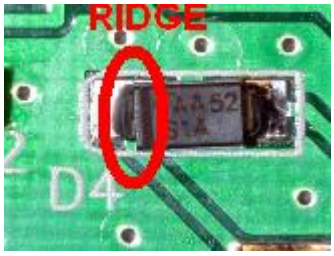


In addition, Q1 and Q2 are physically small devices, soldered to small pads. Do not overheat during installation or the devices may be damaged or, worse yet, the pads may lift from the fiberglass substrate.

❑ Install Q1, a J310 type NJFET. Q1 is marked 50W. (This may change depending upon the supplier; check the kit packing for an update.)

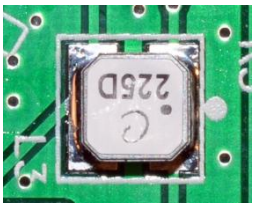
❑ Install Q2, a J271 type PJFET. Q2 is marked 62T. (This may change depending upon the supplier; check the kit packing for an update.)

❑ Install D4, a silicon power diode, marked S1A. Note D4 has a ridge molded into one end of the housing.



The ridge end of D4 is oriented as illustrated in the photograph; it is at the "D4" end of the silk screen where the component outline has angled edges.

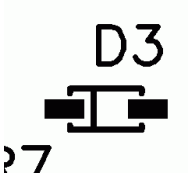
❑ Install L3, a 2m2 RF choke, marked 225D.



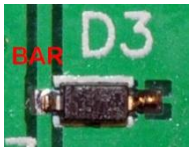
Note that L3 has a dot on the label and a corresponding dot on the PCB silk screen. Install L3 so that the dots are aligned as illustrated.

When installing L3, tack one edge in place whilst holding it in position. Solder the opposite pad. Then return to the original pad and resolder.

❑ Install D3, a 1N4148 type diode. This diode may have various markings depending upon the supplier but it has a distinctive appearance that cannot be confused with other parts contained in this kit. As of the writing of this manual, these parts are marked 5H.



One end of the diode will have a ridge or bar molded into the housing. D3 is oriented so that the ridge is on the end where the silk screen line is shown. In the photos, D3's bar will be at the left side of the image.



D1 and D2 are optional components. If your Z10130A will be exposed to strong electric fields, such as from a nearby amateur radio transmitter, you may wish to install D1 and D2. These two diodes are arranged as an input limiter to protect Q1 and Q2 from overload when power is applied to the Z10130A. (When power is removed, relay K1 grounds Q1 and Q2's inputs and places the Z10130A into "safe mode" where nearby transmitters will not damage Q1 and Q2. However, if you plan to operate the Z10130A while nearby transmitters are active, you should consider whether D1 and D2 should be installed.



The price paid for installing D1 and D2 is degradation in intermodulation intercept as the diodes are non-linear elements that can and will generate intermodulation products.

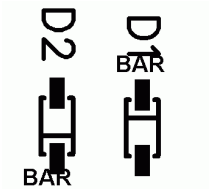
D1 and D2 are 1N4148 type devices, identical with D3, and have the same ridge or bar molded

in the plastic body.

❑ If used, install D1

❑ If used, install D2

Note the ridge or bar side is installed as reflected in the silk screen and the drawing at the right.



❑ Prepare L2, a 20mH common mode power choke for installation.
L2 is marked 203 and has a small ridge molded into the case, adjacent to pin 1.

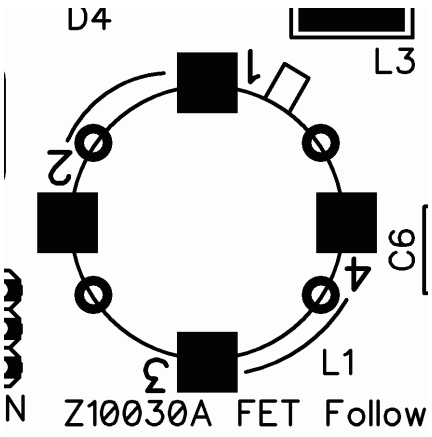


Tin the bottom surface of all four leads with solder. (The bottom surface is the one that is open so that the windings and toroid core are visible.)

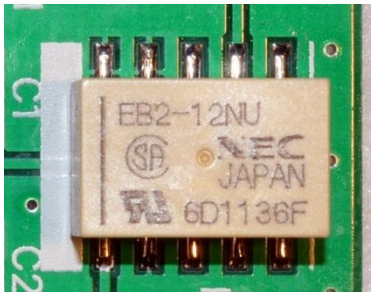
Orient L2 so that its ridge matches the silk screen ridge. The ridge should point towards L3.

Hold L2 so that its four leads are centered on the pads, tack solder one pad.

Recheck the alignment of L2 on the pads, twisting it slightly if necessary or realigning. Solder the remaining pads and touch up the first tacked pad.



❑ Install K1, a DPDT 12V relay.



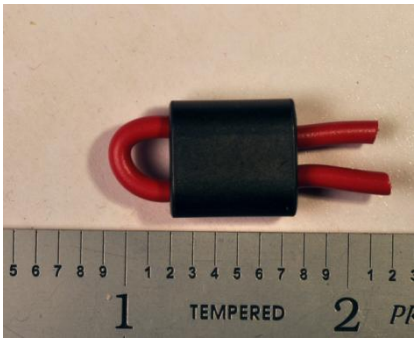
The relay is oriented so that the thin bar on the relay body is at the end of the silk screen identified with a thick white bar, as illustrated in the photograph.

Align the relay so that it is centered on the pads. Hold the relay in place and solder one corner pad. Recheck the alignment and solder the diagonally opposite corner pad. Solder all remaining pads.

❑ Install SA1, a spark gap high voltage arrestor.

This part can be difficult to install. First, generously tin SA1's non-grounded pad. Holding SA1 with tweezers, melt the solder on the tinned pad and mount SA1. Allow 30 seconds for the solder to cool. Solder the ground pad in place.

Construct Transformer T1



T1 is a balun that converts the unbalanced output of Q1 and Q2 to a balanced or floating output suitable for twisted pair or twin-lead type transmission line. It is wound on a BN73-202 type core with no. 32 bifilar magnet wire.

T1 is a multi-aperture (binocular) core. When counting turns, remember that one turn requires the wire to pass through both holes. The photo at right shows one complete turn through a binocular core. Passing the wire through one hole counts as one-half of a turn.

T1 is a ferrite core and has sharp edges. To avoid wire damage caused by abrading the enamel insulation during winding, Teflon insert bushings are used.

The magnet wire supplied with the Z10130A is "solder strippable" which means that the insulation will dissolve in molten solder. First wind the transformer and after winding clamp the transformer in place with a soft jaw vise. Cut the lead length to the recommended value and apply the soldering iron to the wire end. Add solder to form a 'blob' of molten solder. After a few seconds, the insulation will begin to dissolve. Work the soldering iron along the wire, adding fresh solder as necessary to maintain a blob of molten solder. Do not tin right up to the core; tin only to within 1/8th inch (3mm) of the core.

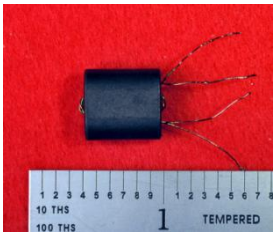


- ❑ Cut two bushings from the length of Teflon tubing. The bushings should slightly extend (between 1/16th and 1/32nd inch [1.5mm to 0.75mm]) from each end of the core when inserted.

  When cutting the Teflon tubing, use a sharp hobby knife or a razor blade. Scissors or dull wire cutters can leave a ragged edge. After cutting, roll the tubing between your fingers to restore it to circularity. Insert the tubing into the core and using a pencil, gently form the ends to a slightly bell or funnel shape as illustrated in the photograph.

  The tubing more or less "self-centers" lengthwise if you first wind 1.5 turns of bifilar wire and gently pull the wire from both ends.
- ❑ Measure 34 inches (850mm) of red and green #32 magnet wire and twist together at approximately 4 twists per inch. (One twist every 6mm) A variable speed electric drill can be used for this task.
- ❑ Wind 16 turns through T1's core. When starting the winding, allow approximately one inch (25mm) of wire to extend from one hole. When winding, make sure that the wire goes through the Teflon tubing. And, remember that a winding must pass through both holes to be counted as a complete turn.

❑ After winding, cut the leads to approximately ¾ inch (16 mm). Untwist the leads for this length and tin. The completed transformer should match the photo.



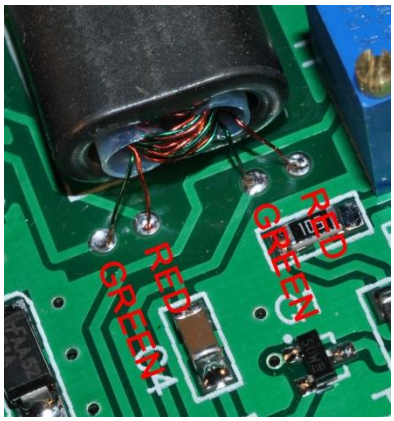
❑ Apply the glue dot to the printed circuit board, centering it in the T1 silk screen outline. This is best done by removing the protective paper from one side and trimming the remaining protective paper to be a square shape around the dot. Firmly press the exposed dot surface onto the PCB. With a quick motion, pull the paper off the top side of the glue dot.

❑ Attach T1 to the PCB, routing the four wires as illustrated in the photograph. Do not solder yet.

Press T1 into the glue dot firmly. From the bottom of the board, gently pull the leads through until they resemble the photograph.

The portion of the lead going through the pads should be free of insulation and tinned. If not, remove any insulation from this portion of the leads using the soldering iron technique earlier described.

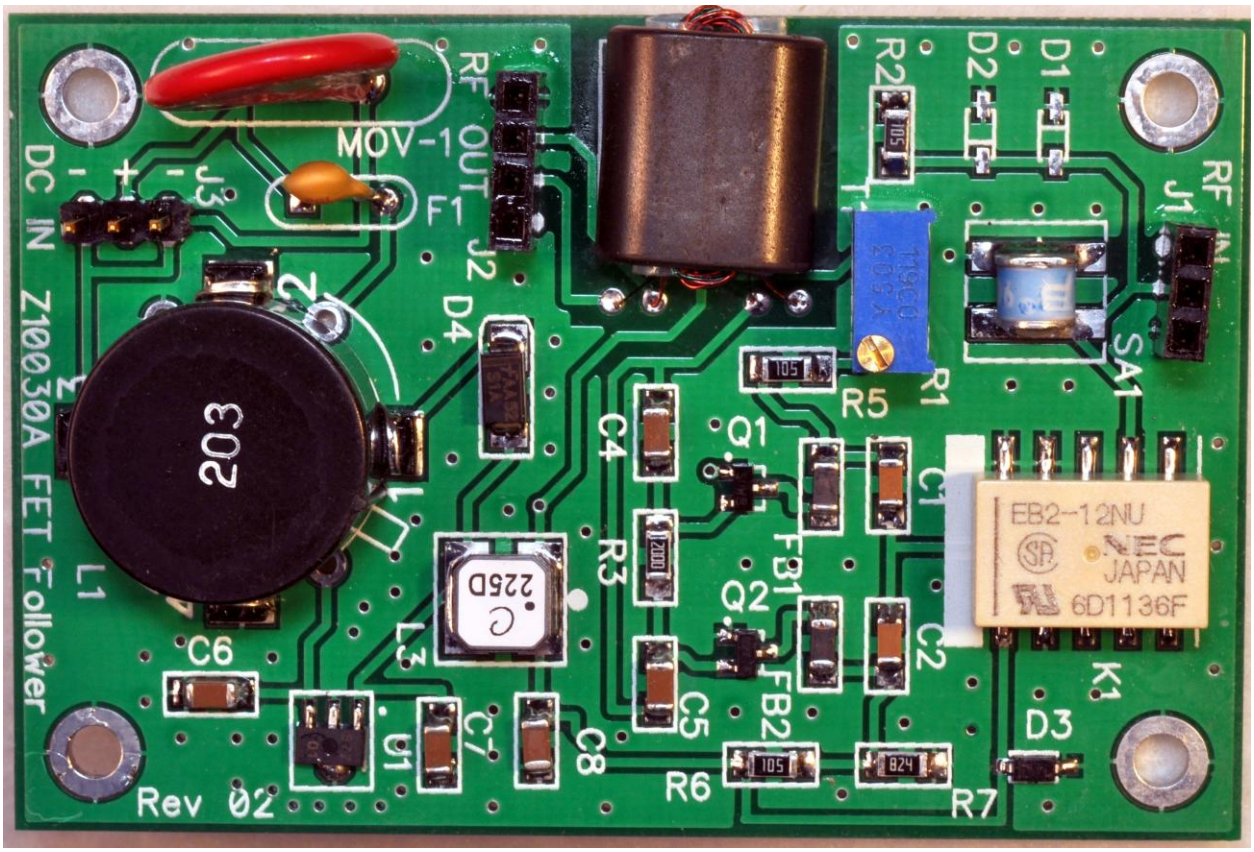
Solder the four leads.



❑ Install J2, a 4-pin female header socket.
❑ Install F1, a 100mA polyfuse, marked XF010.
❑ Install MOV-1, an over-voltage protector. As of the writing of this manual, the part is marked P18Z3, but this may change if a different supplier is used.
❑ Locate the male header pin strip and snap off (or cut with diagonal pliers) a 3-pin section. Install at J3. (Use the 3-pin female header as a tool for holding the 3-pin male section in place.)
❑ Install J1, a 3-pin female header socket.
❑ Install R1, a 50K multi-turn trim pot, marked 503.

Post Assembly Check and Adjustment

This completes assembly of the Z10130A. Please check board for missed solder connections or other errors. The top layer of your board should look like that in the photograph below.



Before applying power to your Z10130A you may wish to make an abbreviated resistance measurement check to located gross errors. An annotated schematic with normal resistance readings is provided in the Troubleshooting section of this manual.

For post-construction checkout, measure the resistance to ground at J3, pin 2 (DC in +) and pins 1 and 3 (DC in -), and the resistance to ground at U1's output. If these are within a reasonable range of the nominal values, proceed to the apply power and adjust R1 procedure.

Adjusting Bias Potentiometer, R1

After assembly, it is necessary to adjust R1 for optimum 2nd order intermodulation performance. (3rd order intermodulation performance is only slightly affected by changes in R1's setting.)

This manual provides two methods of adjusting R1, one using laboratory test equipment and one based on off-the-air signals.

Although the test equipment procedure is repeatable, it may not necessarily yield the best performance when the Z10130A is installed with an antenna. This is a consequence of the input signal source

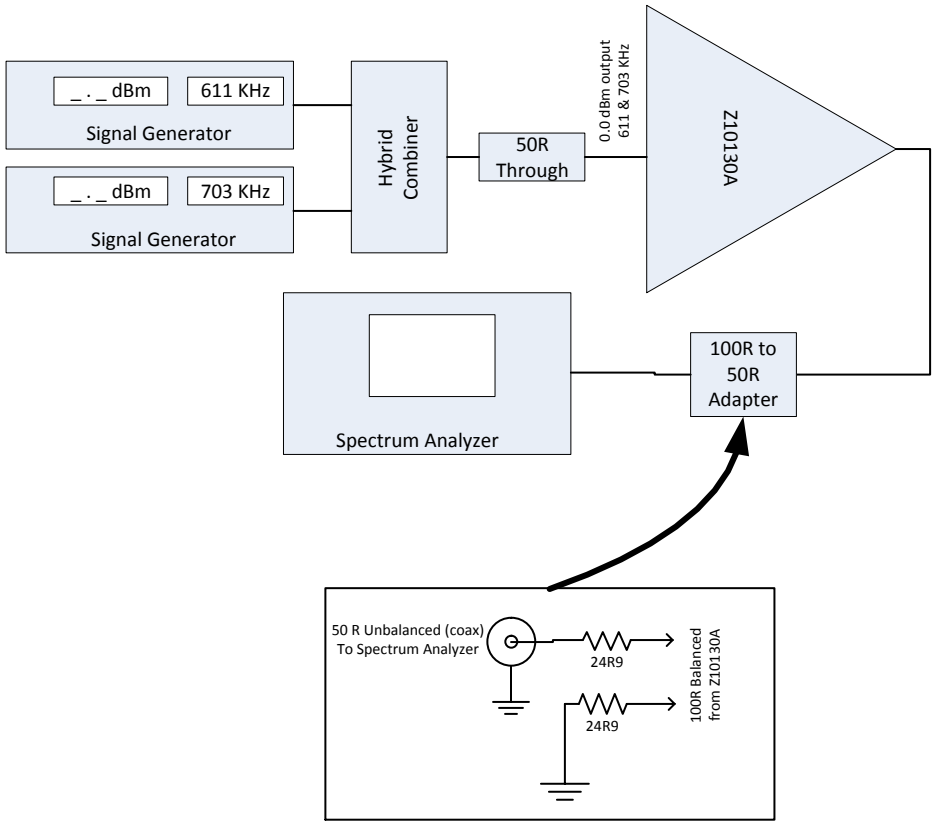
impedance interacting with the amplifier so that the optimum bias adjustment varies to some degree with the signal source impedance.

Laboratory Method

The test setup used at Clifton Laboratories is illustrated in the block diagram below. It is a conventional 2nd and 3rd order intermodulation measurement arrangement, with two test tones applied to the device under test and the intermodulation products measured with a spectrum analyzer.

Since the Z10130A has an output impedance of 100 ohms, and the spectrum analyzer is a 50 ohm input device, a simple resistive matching arrangement is used. It consists of two 24.9 ohm resistors in series with the Z10130A's balanced output, which introduces 6.0 dB loss due to the 2:1 voltage divider.

The discussion assumes familiarity with measuring 2nd and 3rd order intermodulation products.



100R to 50R Adapter

Summary of Protocol

1. Connect hybrid combiner to spectrum analyzer and adjust each of the two test signals (611 KHz and 703 KHz) to 0.0 dBm.

2. Connect the hybrid combiner output to the Z10130A input, using a 50 ohm "through" at the Z10130A's input. (A 50 ohm "through" can be jury rigged as a 50 ohm shunt resistor to ground temporarily installed on the Z10130A's input.)
3. Connect the Z10130A's output to the spectrum analyzer using the 100R-50R adapter. Apply 13.8 DC to the Z10130A's input.
4. The four intermodulation product frequencies are:

Frequency (KHz)	Order
1314	2nd
795	3rd
519	3rd
92	2nd

5. In observing intermodulation products, it is important to ensure the test setup is not the limiting factor. In the case of a spectrum analyzer, a quick check for intermodulation products generated inside the SA is to observe the product level whilst increasing input attenuation. If the intermodulation product is generated outside of the SA, it will reduce level dB for dB as the input attenuation is increased. Intermodulation products generated inside the spectrum analyzer will decrease at a faster rate; 10 dB increase in input attenuation will theoretically reduce internally generated 2nd order products 20 dB and 3rd order products 30 dB.

   Accordingly, sufficient input attenuation should be used in the SA such that it does not contribute internally generated intermodulation products. It may be necessary to use trace averaging to accurately measure intermodulation products at high attenuation settings.
6. Minimize the 2nd order product at 1314 KHz by adjusting R1. At Clifton Laboratories, an HP 8568B spectrum analyzer is used, set to 10 Hz RBW, 10 Hz VBW, zero span during the adjustment process. The signal generators and spectrum analyzer are locked to a common GPS-disciplined time base to avoid frequency error.
7. Switch the spectrum analyzer to 500 Hz span and measure the four intermodulation product signal levels in dBm. Also measure the signal levels of the 611 and 703 KHz test tones. (The two test tones should be substantially identical in level, within a couple tenths of a dB, if step 1 has been correctly performed.)

Frequency (KHz)	Measured Level (dBm)	Order
611		Tone 1
703		Tone 2
1314		2nd
795		3rd
519		3rd
92		2nd

8. To compute the input intercept performance:
   a. Compute the difference between the test tone level (611 and 703 KHz) and each of the four intermodulation products. For example, 611 and 703 KHz are measured at -10.0 dBm, and 1314 KHz 2nd order product is measured at -110.0 dBm. The difference is: -10.0 –(-110.0) = +100 dB.

b. Complete the difference calculations for all four intermodulation products.

Frequency (KHz)	Measured Level (dBm)	Difference (dB)	Order
611			Tone 1
703			Tone 2
1314			2nd
795			3rd
519			3rd
92			2nd

c. Compute the output intercepts.

i. For 2nd order products, the output intercept equals the test tone level plus the measured difference. For example, test tones = -10.0 dBm, difference is +100 dB, output intercept (OIP2) = -10 dBm + 100 dB = +90.0 dBm

ii. For 3rd order products, the output intercept equals the test tone level plus one half the measured difference. For example, suppose 795 KHz intermodulation product is -96.2 dBm. The difference (step 8(a)) is -10.0-(-96.2)= +86.2 dB. The output intercept is thus -10 dBm + 86.2 dBm/2 = +33.1 dBm.

iii. Complete the table below

Frequency (KHz)	Measured Level (dBm)	Difference (dB)	Output Intercept (dBm)	Order
611				Tone 1
703				Tone 2
1314				2nd
795				3rd
519				3rd
92				2nd

9. To convert to input intercepts, add the Z10130A net gain. The net gain is the Z10130A's amplifier gain and the loss of the 100R to 50R matching resistors. The net gain is measured as the difference between the input signal (0.0 dBm) and the signal level of the test tones measured at the spectrum analyzer input (approximately -10 dBm), for a resulting net gain of -10 dBm.. For example, the 2nd order output intercept is +90 dBm. The input intercept is thus +90 dBm -10 dB = +100 dBm. Complete the table for the four input intercept values.

Frequency (KHz)	Measured Level (dBm)	Difference (dB)	Output Intercept (dBm)	Input Intercept (dBm)	Order
611					Tone 1
703					Tone 2
1314					2nd
795					3rd
519					3rd
92					2nd

Off the Air Method

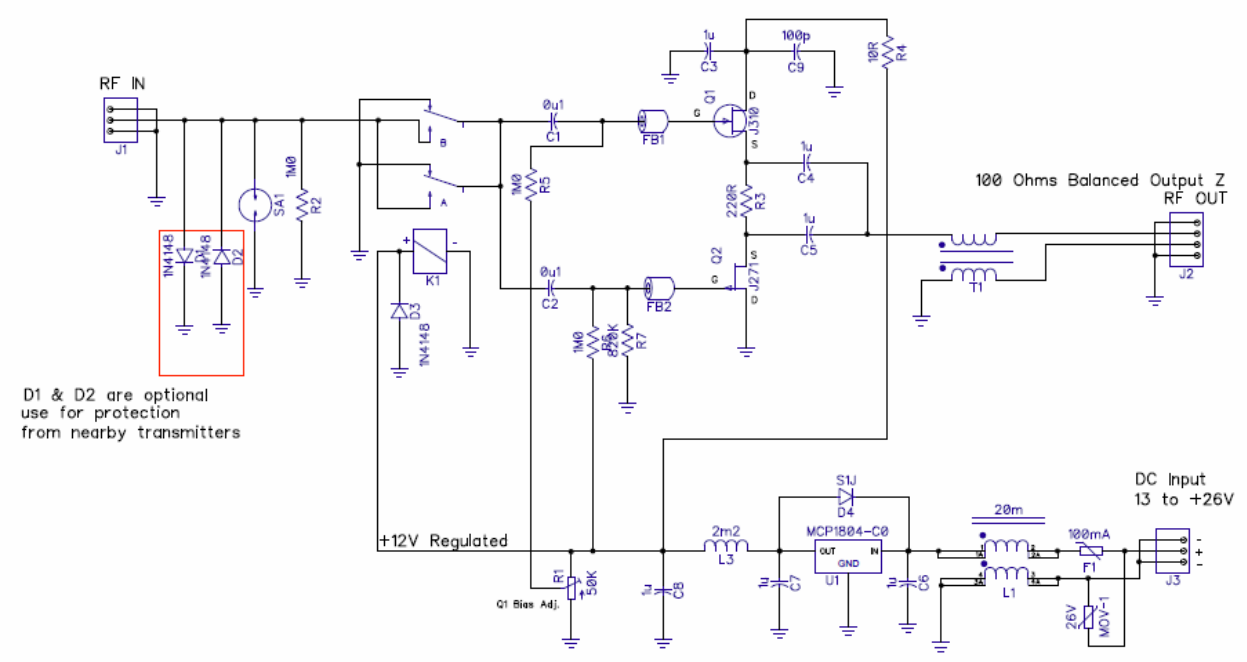
For builders without access to laboratory test equipment, R1 may be adjusted using off-the-air medium wave band signals. Dr. Lankford has provided the following methodology (edited from a series of E-mail messages):

1. Using a temporary antenna
    a. A reasonably strong signal must be applied to the amplifier to generate intermodulation products. A suitable temporary adjustment antenna is about 100 feet (30 meters) of insulated wire running out my window and onto the ground in my front yard in a straight line connected to the amplifier input. The ground plane of the FET follower is grounded to an outdoor ground, so the antenna is a "noise reducing WOG."
    b. Adjustment is made at night when there are plenty of strong MW signals. Adjust the bias potentiometer, R1, all the way in one direction, I think to max gate voltage (you can hear my pot "click" when the adjust screw is turned to the end). MW intermodulation products can be heard all over the place above 2 MHz, every 10 kHz. I assume it was 2nd order because the FET follower IIP3 is high regardless of the pot settings. I tuned to a strong intermodulation product at 2910 kHz and chose that as the frequency to set the bias pot. The exact frequency of the intermodulation product will, of course, depending upon the medium wave frequencies in use at any particular site. (I turned on the BFO so that I could hear the IMD2 better as it disappeared into the noise.) Started turning the pot screw adjust counter clockwise. After quite a few turns, the intermodulation product started going down. When it disappeared I started counting turns. There were 11 turns before the intermodulation product appeared again. Turned a few extra turns to be sure. Then turned the screw adjust clockwise until the IMD disappeared again, turned 5 and a half more clockwise turns, and stopped. The FET follower should now be adjusted for max IIP2.
2. Using the final antenna
    a. The optimum bias potentiometer setting depends to some degree upon the antenna connected. The FET Follower IIP2 can be maximized for any antenna if one uses two walkie-talkies, one at the speaker of the receiver in the house, the other with the person adjusting the R1 25-turn pot at the antenna with the FET follower connected to one of the antenna elements that will be used (either as a stand-alone antenna or as one part of an array).
    b. As described in Step 1.b, Set up the FET Follower attached to the desired antenna element with the 25 turn pot set to one of the extremes. Tune around above 2 MHz until you find the strongest IMD2 you can find. Most walkie-talkies have a VOX (voice operated transmit) function. With VOX enabled, turn on the walkie-talkies with one of the set up against the receiver speaker. Go outside to the FET follower with the other walkie-talkie and adjust the pot as described at 1.b. (The particular walkie-talkies I use are Midland GTX Xtra Talk models.)

Theory of Operation

The Z10130A is based upon Dr. Dallas Lankford's publication "Complementary J310 – J271 FET Follower, 8/21/2011, rev 2/5/2012" and as such is intended to be used with the antennas Dr. Lankford has designed and documented, such as the Q45 and Q90 arrays.

The Z10130A implementation of his design is presented below.



The heart of the circuit is Q1 and Q2, comprising a complementary symmetry follower using J310 NJFET and J271 PJFET devices. To optimize 2nd order intermodulation performance, Q1's gate bias is made adjustable through R1, a 50K multi-turn trimmer potentiometer. Q2's gate voltage is fixed at approximately 5.40V by the R6/R7 voltage divider. Q2's gate-to-source bias voltage is function of R6/R7, the IR drop across R3 and the drop across Q1.

R4, C3 and C9 de-couple Q1's Vdd supply.

The input circuit is routed through a relay K1 that disconnects the antenna and grounds the FET gates when power is removed. This reduces the risk of damage from static electricity or nearby lightning strikes when power is removed. R2 is a static drain resistor, and SA1 is a 90V spark gap device. SA1 is not intended to protect Q1 and Q2 from damage but rather to reduce damage to devices connected downstream of the Z10130A.

Diodes D1 and D2 are optional clamping diodes to limit the RF voltage seen by Q1 and Q2 from nearby transmitters. They should be used only if the Z10130A will be exposed to nearby amateur radio transmitters or the like, as otherwise the Z10130A's intermodulation performance may be degraded due to the diode non-linearity.

Output voltage is coupled from Q1 and Q2 via blocking capacitors C4 and C5 and fed to a ferrite core balun, T1. The recommended impedance the Z10130A should be operated into is 100 ohms. T1 has a 1:1 turns ratio and does not transform impedance but does converted the single ended output of Q1 and Q2 to a balanced output.

DC operating voltage is supplied through a common mode choke, L1, and a 12V output low dropout regulator, U1. L3 and C8 reduce U1's broadband output noise that would otherwise be coupled into Q1 and Q2 through the gate bias network. U1 is a Microchip MCP1804 device, chosen for low broadband noise output as well as other operating parameters. C6 and C7 are selected based upon ESR to ensure U1's stability.

L1 is a 20mH common mode choke to reduce unwanted signal ingress over the power feeder. F1 is a 100 mA polyfuse to protect the power feeder and power source from a short circuit within the Z10130A circuitry. MOV-1 is a metal oxide varistor that clamps the power feeder voltage. As with SA-1, MOV-1's purpose is not to protect the Z10130A's components but rather to reduce damage to downstream devices that may be connected to the Z10130A's DC power feeders.

Connections and Operation

Connection and operation of the Z10130A is covered in Dr. Lankford's publications:

- An Active QTFA 90, Dallas Lankford, 2/6//2012
- Q25 Active MW Array Tests, Dallas Lankford 12/8/2011
- Q45 Active Array, Dallas Lankford, 11/17/2011, rev. 12/3/2011
- Q45 Active MW Array Tests Summary, Dallas Lankford, 11/17/2011, rev. 12/14/2011
- Q45 Active MW Array Tests, Dallas Lankford, 11/17/2011, rev. 12/10/2011

Troubleshooting

Following are annotated schematics of the Z10130A with:

1. Schematic
2. DC resistance to ground
3. DC voltage
4. AC signal level

The Z10130A is a simple device and experience suggests the most likely components to fail are Q1 and Q2, as they are exposed (when power is applied) to potentially large voltages from nearby lightning strikes or static discharges. The likelihood of damage to Q1 and Q2 can be reduced if protection diodes D1 and D2 are installed, although some degradation in intermodulation performance will be seen for elevated signal levels.

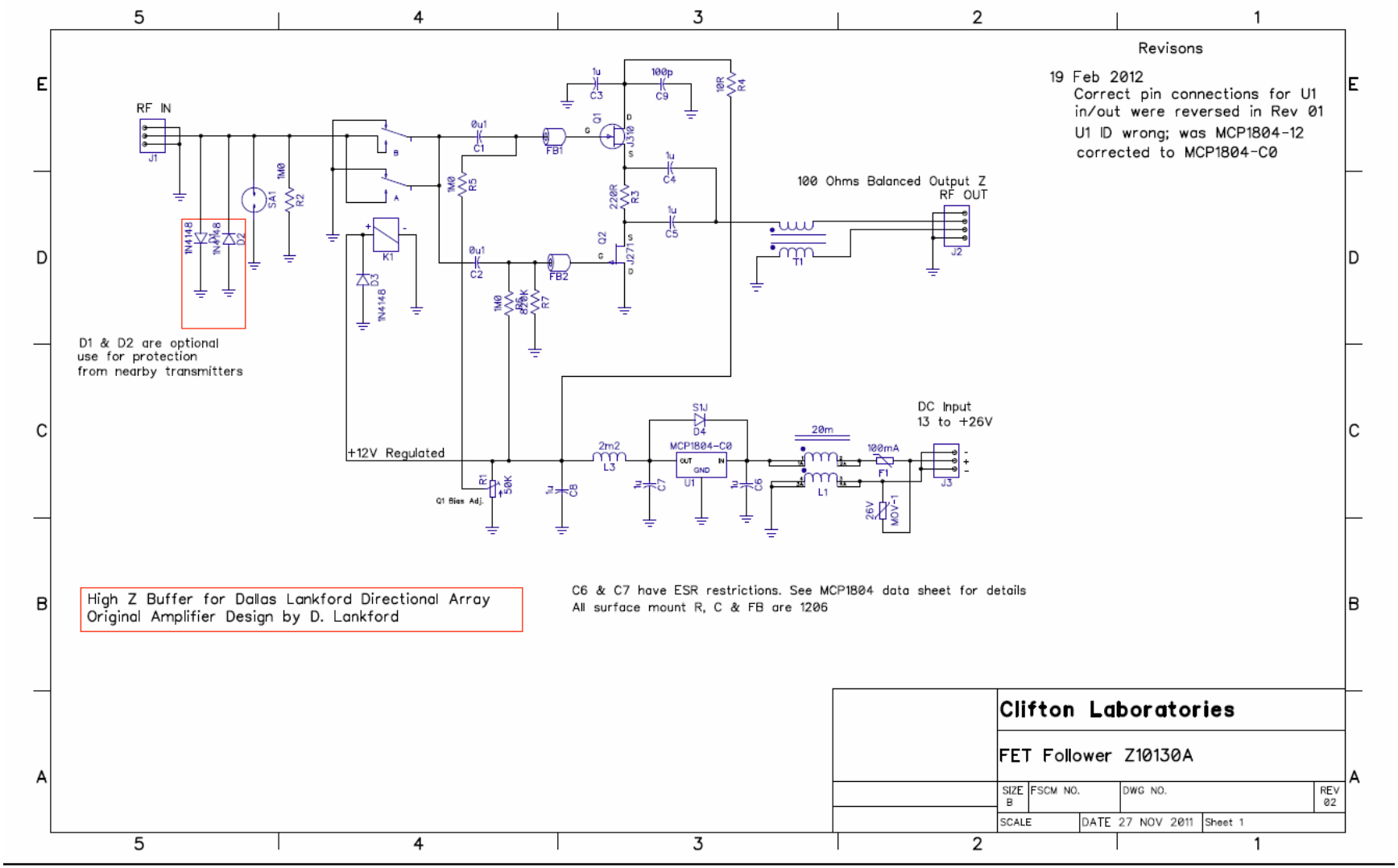
Failure of Q1 and Q2 will usually be evidenced by excessive current draw (greater than 25 mA or so) or reduced current draw (at a level of 10 to 12 mA representing just K1's coil.) The current through Q1 and Q2 may be determined by measuring the voltage drop across R3 and computing the current through ohm's law. I = (voltage drop across R3)/200 ohms. The normal current through Q1 and Q2 is approximately 8 to 10 mA, with the exact value will depend upon device parameters and R1's setting.

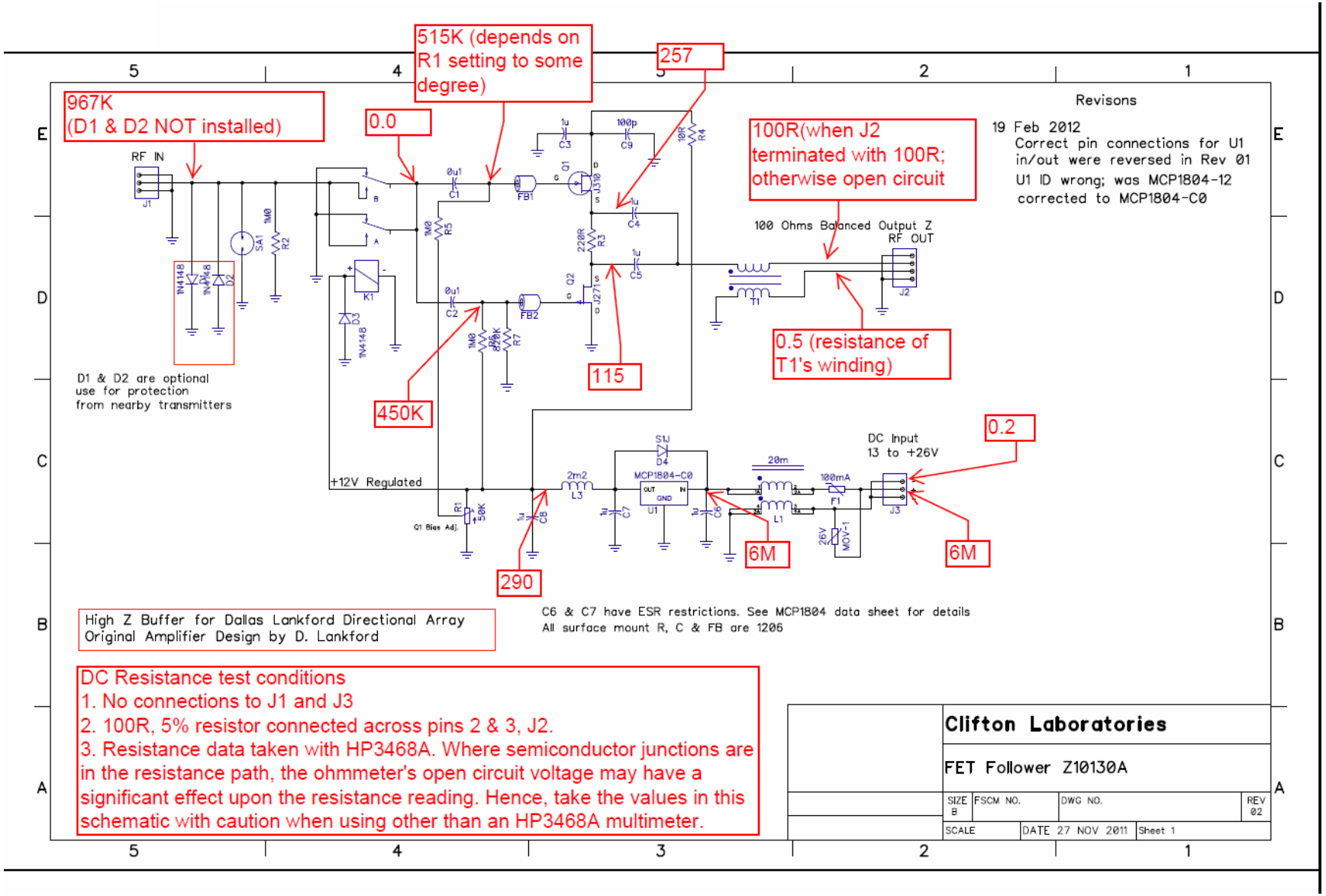
Failure in U1, the voltage regulator will manifest itself by excessive voltage on its output, or a short circuit on its input (which should put polyfuse F1 into a high resistance state) or it may fail as an open circuit.

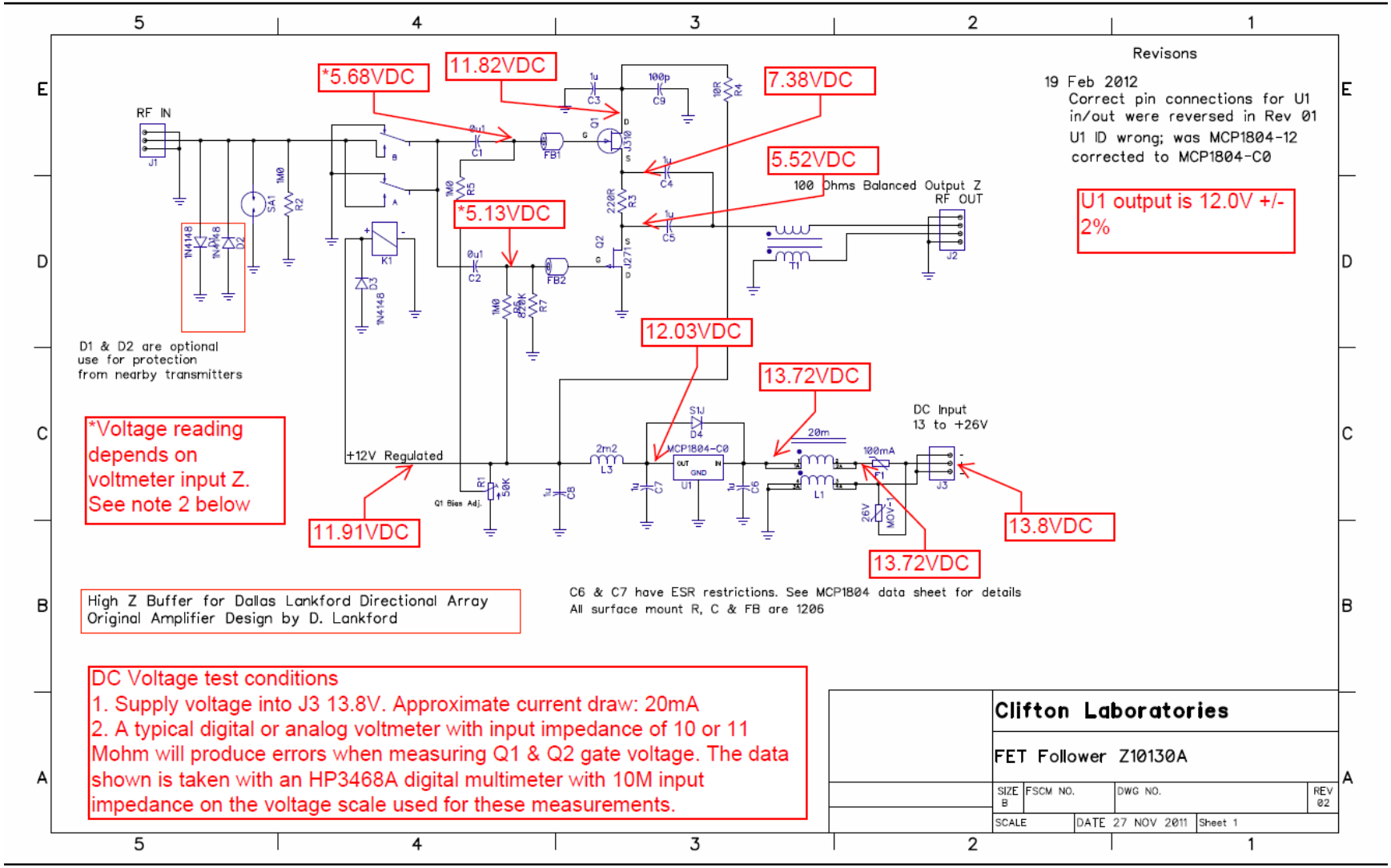
Note that a short circuit on the Z10130A's raw power input bus will manifest itself by a moderately high current draw. Polyfuse F1 will draw sufficient current to maintain itself in the "hot" high resistance mode. This is contrary to a normal one-shot fuse that blows open when subject to overcurrent. F1 will reset itself when the output short circuit is cleared. Depending on the degree of "short" in the short circuit, some voltage will be supplied through F1.

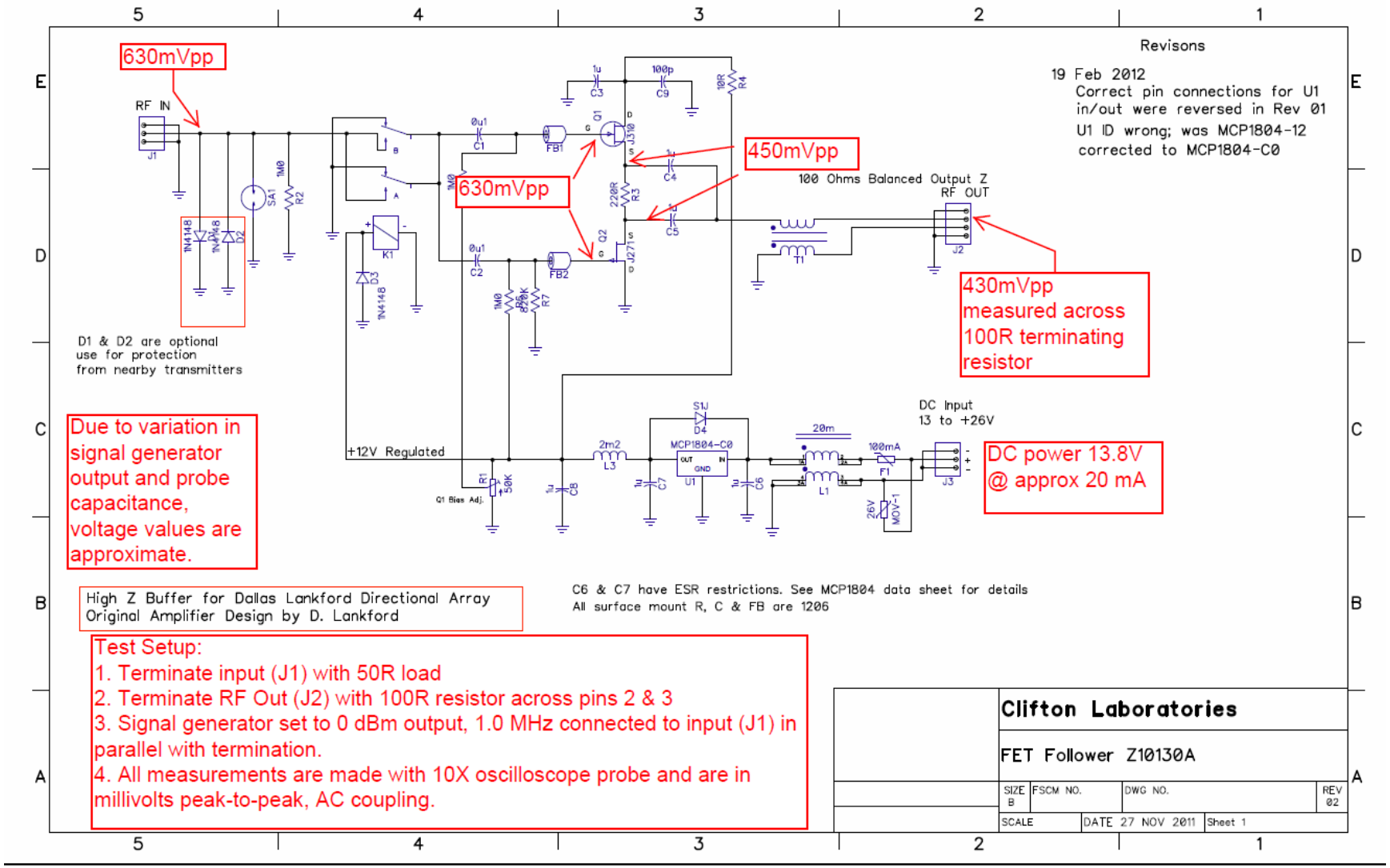
A failure in K1 should be detectible by measuring the armature pins to contact pin resistance.

Note: The schematics in this section show R3 as 220R. A later production change is 200R. The voltage and resistance measurements are for 200R.


Revisons
19 Feb 2012
Correct pin connections for U1 in/out were reversed in Rev 01
U1 ID wrong; was MCP1804-12 corrected to MCP1804-C0
RF IN
J1
100 Ohms Balanced Output Z
RF OUT
J2
T1
D1 & D2 are optional use for protection from nearby transmitters
DC Input
13 to +26V
+12V Regulated
MCP1804-C0
Q1 Bias Adj.
High Z Buffer for Dallas Lankford Directional Array
Original Amplifier Design by D. Lankford
C6 & C7 have ESR restrictions. See MCP1804 data sheet for details
All surface mount R, C & FB are 1206
Clifton Laboratories
FET Follower Z10130A
SIZE B
FSCM NO.
DWG NO.
REV 02
SCALE
DATE 27 NOV 2011
Sheet 1


967K
(D1 & D2 NOT installed)
515K (depends on R1 setting to some degree)
0.0
257
100R(when J2 terminated with 100R; otherwise open circuit
Revisons
19 Feb 2012
Correct pin connections for U1 in/out were reversed in Rev 01
U1 ID wrong; was MCP1804-12 corrected to MCP1804-C0
RF IN
100 Ohms Balanced Output Z
RF OUT
0.5 (resistance of T1's winding)
115
450K
D1 & D2 are optional use for protection from nearby transmitters
+12V Regulated
DC Input
13 to +26V
0.2
6M
6M
290
High Z Buffer for Dallas Lankford Directional Array
Original Amplifier Design by D. Lankford
C6 & C7 have ESR restrictions. See MCP1804 data sheet for details
All surface mount R, C & FB are 1206
DC Resistance test conditions
1. No connections to J1 and J3
2. 100R, 5% resistor connected across pins 2 & 3, J2.
3. Resistance data taken with HP3468A. Where semiconductor junctions are in the resistance path, the ohmmeter's open circuit voltage may have a significant effect upon the resistance reading. Hence, take the values in this schematic with caution when using other than an HP3468A multimeter.
Clifton Laboratories
FET Follower Z10130A
SIZE B
FSCM NO.
DWG NO.
REV 02
SCALE
DATE 27 NOV 2011
Sheet 1


*5.68VDC
11.82VDC
7.38VDC
5.52VDC
*5.13VDC
12.03VDC
13.72VDC
11.91VDC
13.8VDC
13.72VDC
RF IN
RF OUT
100 Ohms Balanced Output Z
+12V Regulated
DC Input
13 to +26V
Q1 Bias Adj.
MCP1804-C0
D1 & D2 are optional
use for protection
from nearby transmitters
*Voltage reading
depends on
voltmeter input Z.
See note 2 below
Revisons
19 Feb 2012
Correct pin connections for U1
in/out were reversed in Rev 01
U1 ID wrong; was MCP1804-12
corrected to MCP1804-C0
U1 output is 12.0V +/-
2%
High Z Buffer for Dallas Lankford Directional Array
Original Amplifier Design by D. Lankford
C6 & C7 have ESR restrictions. See MCP1804 data sheet for details
All surface mount R, C & FB are 1206
DC Voltage test conditions
1. Supply voltage into J3 13.8V. Approximate current draw: 20mA
2. A typical digital or analog voltmeter with input impedance of 10 or 11
Mohm will produce errors when measuring Q1 & Q2 gate voltage. The data
shown is taken with an HP3468A digital multimeter with 10M input
impedance on the voltage scale used for these measurements.
Clifton Laboratories
FET Follower Z10130A
SIZE B
FSCM NO.
DWG NO.
REV 02
SCALE
DATE 27 NOV 2011
Sheet 1

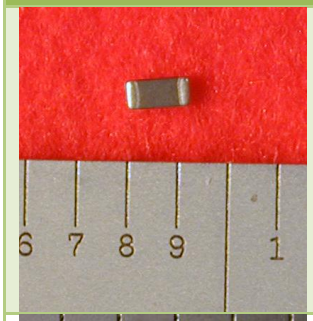
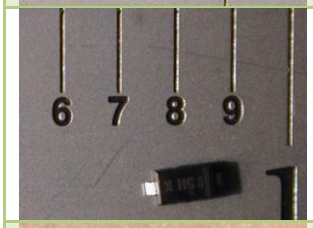
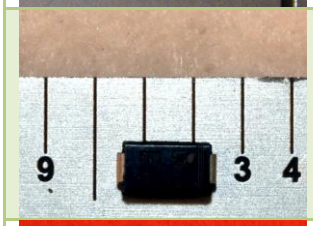
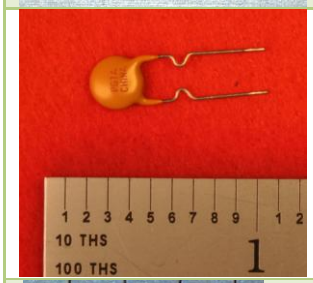
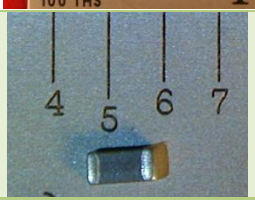

630mVpp
RF IN
J1
450mVpp
630mVpp
100 Ohms Balanced Output Z
RF OUT
J2
430mVpp measured across 100R terminating resistor
D1 & D2 are optional use for protection from nearby transmitters
Due to variation in signal generator output and probe capacitance, voltage values are approximate.
+12V Regulated
DC Input 13 to +26V
DC power 13.8V @ approx 20 mA
MCP1804-C0
Q1 Bias Adj.
C6 & C7 have ESR restrictions. See MCP1804 data sheet for details
All surface mount R, C & FB are 1206
High Z Buffer for Dallas Lankford Directional Array
Original Amplifier Design by D. Lankford
Test Setup:
1. Terminate input (J1) with 50R load
2. Terminate RF Out (J2) with 100R resistor across pins 2 & 3
3. Signal generator set to 0 dBm output, 1.0 MHz connected to input (J1) in parallel with termination.
4. All measurements are made with 10X oscilloscope probe and are in millivolts peak-to-peak, AC coupling.
Revisons
19 Feb 2012
Correct pin connections for U1 in/out were reversed in Rev 01
U1 ID wrong; was MCP1804-12 corrected to MCP1804-C0
Clifton Laboratories
FET Follower Z10130A
SIZE B
FSCM NO.
DWG NO.
REV 02
SCALE
DATE 27 NOV 2011
Sheet 1

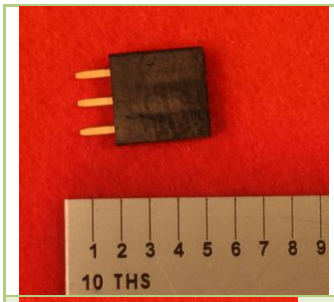
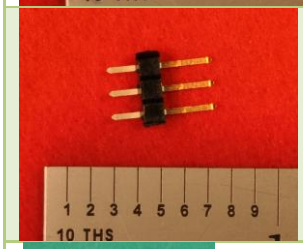
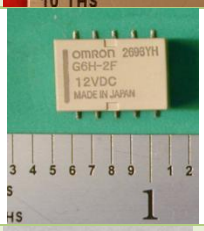
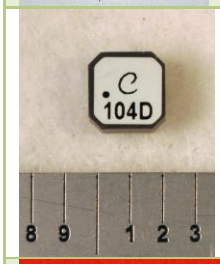
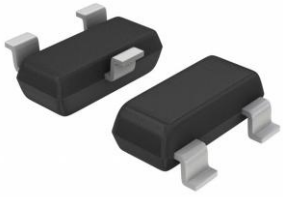
Parts List

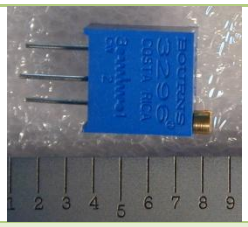
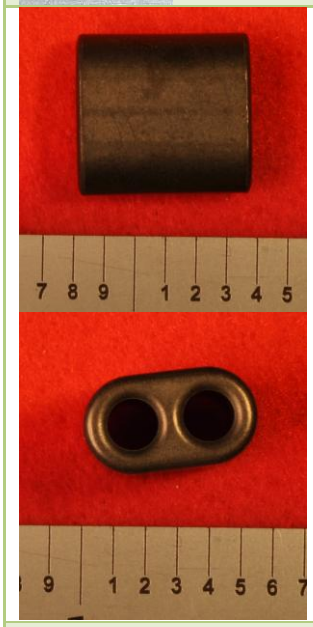
The scale in the photograph is marked in inches and tenths of an inch (2.54mm).

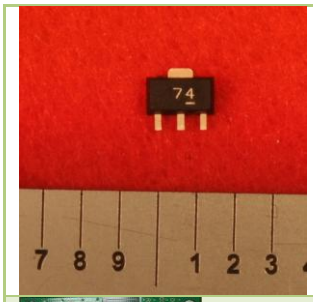
Surface mount parts without identifiers are packed in labeled coin envelopes. To avoid mixing up components, be careful when opening the envelopes and handling the parts.

Parts values in this manual are identified with the decimal point indicated by the multiplier digit. For example a 10.0 ohm resistor is identified as 10R0, a 1.0uF capacitor as 1u0, etc.

Photo	Component ID	Value	Marking	Quantity
	C3, C4, C5, C6, C7, C8	1uF, X7R, 50V 1206 ceramic capacitor	None	6
	C1, C2	0u1, X7R, 100V 1206 ceramic capacitor	None	2
	C9	100pF, C0G 50V 1206 ceramic capacitor	None	1
	D1, D2, D3	1N4148 Silicon signal diode surface mount	Varies	1
	D4	D1A, silicon diode 1A forward, 50V PIV	D1A	1
	F1	100mA polyfuse	RXEF010 or RXEF010S	1
	FB1, FB2	Parasitic suppression ferrite beads	None	2

	J1 and mating connector for J3 J2 (J2 is a 4-pin version-not pictured)	3 position, 0.1 inch spacing single row, 0.025 inch square pin header socket; J2 identical except for 4 pins.	None	2 1x3 1 1x4
	J3 and mating connectors for J1 and J2 -- header pins (male)	0.1 inch single row male header pins. Snap apart at indentation or cut with side cutting pliers.	None	10
	K1	DPDT signal type relay, 12V coil.	Various, including G6H-2F, EB12-NU	1
	L1	20mH common mode choke	203	1
	L2 (pictured example is not labeled the same as the part used in Z10130A.)	2m2 inductor	225	1
	MOV-1	Voltage clamping metal oxide varistor	Various, including: 180M V18AZ3P	1
	Q1	J310 type surface mount NJFET	50W	1
	Q2	J271 type surface mount PJFET	62T	1

	R1	50K ohm multi-turn trim pot	503	1
	R2, R5, R6	1M0 1206 resistors, either 1% or 5% tolerance	105 (if 5%) 1004 (if 1%)	3
	R7	820K 1206 resistor, either 1% or 5% tolerance	824 (if 5%) 8203 (if 1%)	
	R3	200R 1% 1206 resistor	2000	1
	R4	10R0 1% 1206 resistor	10R0	1
	SA1	Gas tube over-voltage protector	Color and marking may vary depending on manufacturer	1
	T1	BN-73-202	None	1

	U1 (device pictured has a different marking but is otherwise identical with U1.)	MCP1804-C0 12V low dropout regulator	97Z	4
	Printed Circuit Board		Z10130A and PCB revision	1
None	Wire	No. 32 red & green	None	40” (1m) each color
	Teflon Bushing	1.5” (38mm) 0.103” ID		1
None	Adhesive dot			1