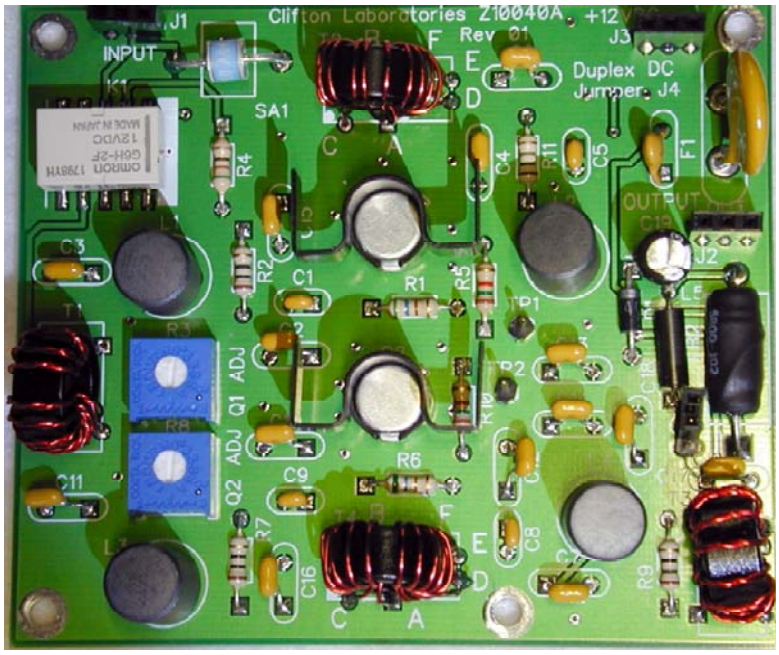
Z10040A
Broadband Norton Amplifier

Assembly and Operation Manual



Version 0.1 May 2009

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Model Z10040A Broadband Norton Amplifier

Version 0.10 2009

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Last Revised 10 May 2009

Trademarks and Copyright

Material in this document copyrighted © 2009 Clifton Laboratories. All rights reserved. It is provided to allow the Z10040A purchasers to maintain their equipment and such other purposes as may not be prohibited by law.

Warranty

This warranty is effective as of the date of first consumer purchase.

What is covered: During the ninety (90) days after date of purchase, Clifton Laboratories will correct any defects in the Z10040A due to defective parts or workmanship (if purchased as an assembled unit) free of charge (post-paid). You must send the unit at your expense to Clifton Laboratories, but we will pay return shipping. Clifton Laboratories' warranty does not extend to defects caused by your incorrect assembly or use of unauthorized parts or materials or construction practices.

What is not covered: If the Z10040A is purchased as a kit, this warranty does not cover correction of assembly errors or misalignment; repair of damage caused by misuse, negligence, or builder modifications; or any performance malfunctions involving non-Clifton Laboratories accessory equipment. *The use of acid-core solder, water-soluble flux solder, or any corrosive or conductive flux or solvent will void this warranty in its entirety.* Damage to the Z10040A or equipment connected to it caused by lightning strikes is not covered under the warranty. Whether purchased as an assembled unit or as a kit, also not covered is reimbursement for loss of use, inconvenience, customer assembly or alignment time, or cost of unauthorized service.

Limitation of incidental or consequential damages: This warranty does not extend to non-Clifton Laboratories equipment or components used in conjunction with our products. *Any such repair or replacement is the responsibility of the customer. Clifton Laboratories will not be liable for any special, indirect, incidental or consequential damages, including but not limited to any loss of business or profits.*

Under no circumstances is Clifton Laboratories liable for damage to your equipment connected to the Z10040A resulting from use of the Z10040A, whether in accordance with the instructions in this Manual or otherwise.

Safety Information

The Z10040A operates with a user-supplied DC power supply of 13 to 15 Volts at 100 to 120 mA. The Z10040A, although designed as a low signal level preamplifier, is capable of RF output power approaching the 1 watt level. This output power is capable of damaging receivers or the receiver section of a transceiver or test equipment. It is the user's responsibility to ensure that the Z10040A is properly connected to whatever devices it will be used with.

The Z10040A has no replaceable fuses; rather a self-resetting polyfuse limits short circuit current to approximately 200 mA.

The Z10040A is designed to be used only with receive-type power levels. It should not be used with transmitting equipment. The Z10040A's maximum permitted input RF power is 100 mW (+20 dBm). *Power in excess of this level may damage the Z10040A or equipment connected to it, or both. In addition, since the Z10040A has appreciable gain, output power levels sufficient to damage connected equipment may occur with input signal levels well below +20 dBm.*

Although the Z10040A contains protective measures, all of these protection measures assume that the Z10040A is properly grounded and that good engineering practices have been used in its installation and construction of the ground system. The Z10040A is not intended to survive a direct lightning strike to an antenna connected to its input, whether powered up or not. However, the protective measures incorporated into the Z10040A's design should aid in reducing damage.

General Information and Specifications

Description

The term "Norton Amplifiers" refers to a class of transformer feedback amplifiers developed by Dr. David Norton and described in his US Patent No. 3,891,934, granted June 24, 1975 and now in the public domain. (A copy of Dr. Norton's patent is Appendix C to this Manual.) A Norton amplifier permits the distortion reducing benefits of negative feedback to be applied without impairing the amplifier's noise figure. Hence, Norton amplifiers are also known as "noiseless feedback" amplifiers.

The Z10040A is a broadband (50 KHz to 30 MHz) Norton-style amplifier providing 11 dB gain (other gain values are possible) with very high 3rd order and 2nd order intermodulation intercepts, IP3 and IP2, respectively, with a noise figure of approximately 3.5 dB. The Z10040A is designed for either indoor or outdoor use, with DC power supplied through either separate connections or duplexed over the output coaxial cable. Optional indoor and outdoor die cast enclosures are available for the Z10040A.

The Z10040A is derived from the Norton Amplifier developed by Dr. Dallas Lankford and described in his publication *Common Base Transformer Feedback Norton Amplifiers*, dated 8 June 1994, revised 21 May 2007, available at http://www.kongsfjord.no/dl/Amplifiers/Common%20Base%20Transformer%20Feedback%20Norton%20Amplifiers.pdf.

The Z10040A modifies Dr. Lankford's design in several respects:

- Automatic input disconnect upon DC power removal along with over-voltage gas trap protection
- Improved performance below 500 KHz.
- Over voltage and reverse voltage protection on the DC Power.
- DC power either separately or duplex power.

Clifton Laboratories also offers the Z1202A DC power injector usable with the Z10040A to provide DC power over the coaxial cable.

The Z10040A is available as a kit, including a double sided, silk screened solder masked printed circuit boards and all electronic parts or as an assembled and tested printed circuit board. Options include an indoor die cast enclosure or an outdoor weatherproof die cast enclosure with BNC, UHF or Type N connectors.

Specifications

Parameter	Value
PCB Dimensions	3.00" x 3.50" x 0.75" vertical clearance required. (76.2mm x 88.9mm x 19mm). Four mounting holes for 4-40 screws provided, template in Appendix B.
DC Power Required	Maximum: 15V Minimum: 13.8V Negative to ground, typical DC current 80-100 mA depending on bias adjustment.

Maximum RF Power Input	Do not exceed 100 milliwatts (+20 dBm). IP3 performance specifications are based upon -10 dBm signal input; performance not warranted at greater input levels.
Test Conditions	Performance data is for a 1:11:4 turns ratio design, 13.8 VDC after adjusting balance trimpots for minimum 2nd harmonic distortion. Unless otherwise indicated, performance measurements are made with direct DC power, not duplexed. Figures stated as "typical" are not warranted.
3 dB Bandwidth	100 KHz – 30 MHz. Typical bandwidth 75 KHz - 45 MHz
3rd Order Intermodulation Intercept	+38 dBm. Measured at 12 MHz, input signal level -10 dBm. **PROVISIONAL NUMBER**
2nd Harmonic intercept	+60 dBm. Measured at 5.4 MHz, input signal level -3 dBm. **PROVISIONAL NUMBER**
Gain	11 dB nominal at 1 MHz.
1 dB Gain Compression	+19 dBm input.
Noise Figure	To be measured. Estimated NF less than 4 dB.
Input VSWR	When terminated with 50 ohm load, input VSWR is less than 2:1 over the range 300 KHz – 30 MHz, and is typically below 1.5:1 over this range.

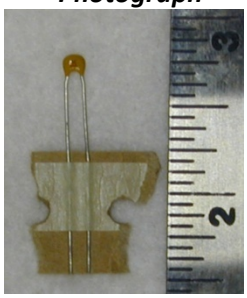
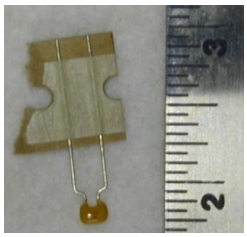
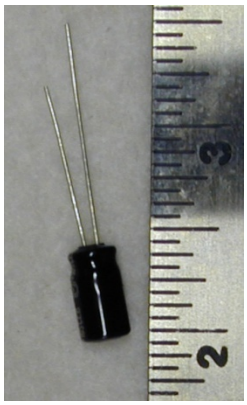
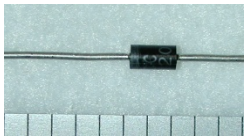
Assembly

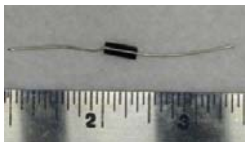
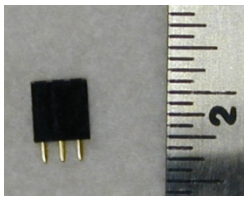
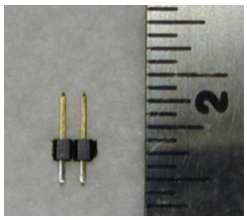
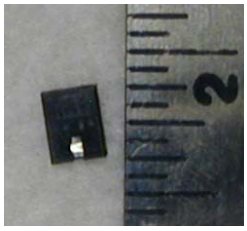
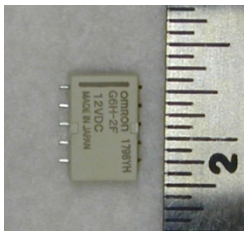
Parts Provided

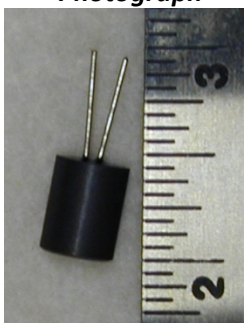
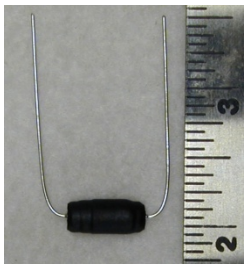
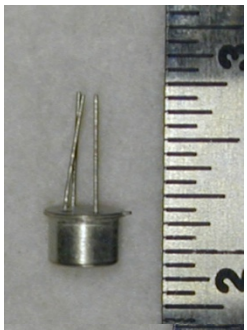
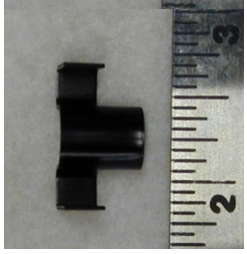
Before starting your build, please take a moment and inventory the parts provided against the list below. The ruler is marked in inches and and 1/16th fractions.

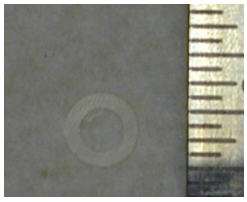
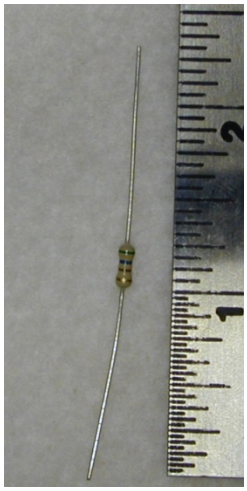
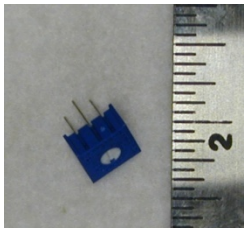
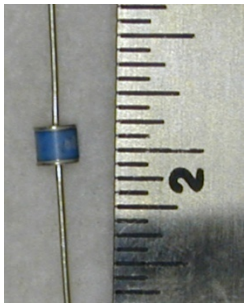
A note on how component values are identified in this manual

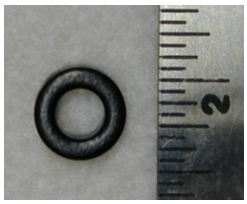
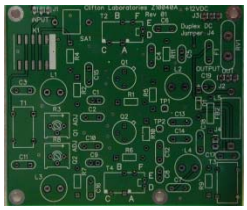
This document follows the international practice of using the value multiplier to indicate the decimal point. Thus, a 1.0µF capacitor is identified as 1µ0 and a 10,000 ohm resistor is identified as 10K0.

Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	4	C1, C5, C8, C9	1000pF leaded ceramic capacitor. Lead spacing 0.1 inches.	102
	14	C10, C11, C12, C13, C14, C15, C16, C17, C18, C2, C3, C4, C6, C7	1u0 leaded ceramic capacitor. Lead spacing 0.2 inches.	105
	1	C19	33u 63V electrolytic capacitor. This component is polarized. Polarity is identified by two methods. The negative lead is the shorter one and the negative lead is marked with a negative symbol on the capacitor case. The longer lead is the positive lead.	33uF 63V
	1	D1	Silicon diode, 1A or greater, 100V or greater. Typically a 1N400x part	1N400x where X may be any number from 0 to 7

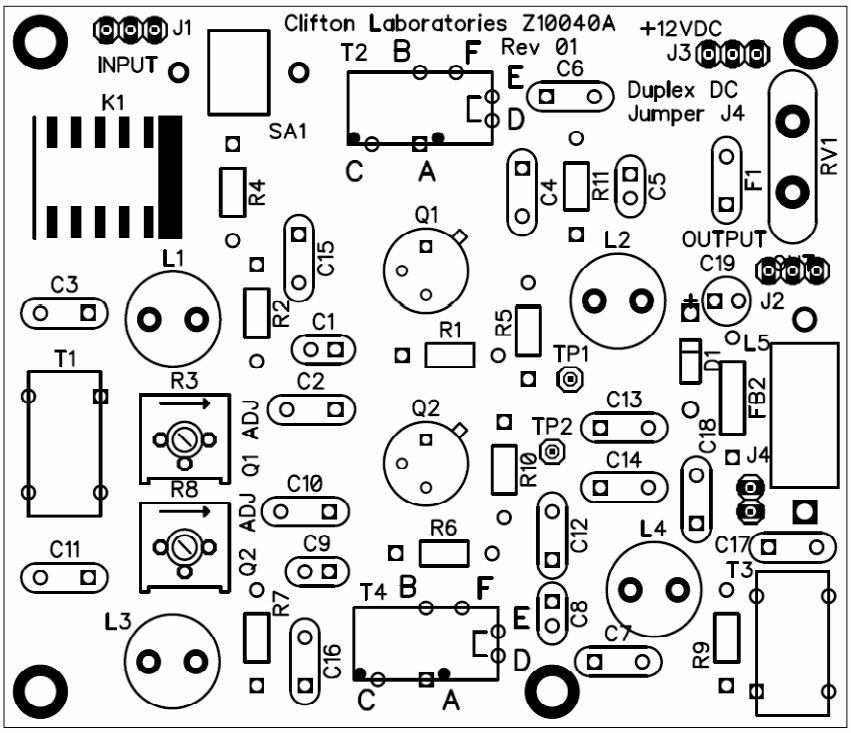
Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	1	F1	200 mA Raychem “polyfuse” PTC varistor.	XF020
	1	FB2	Ferrite bead [FB1 designator is not used]	No marking
	3	J1, J2, J3	3 place 0.1 inch header sockets	None
	1	J4	2 place 0.1 inch header pin May be supplied as a multiple pin strip to be broken as needed by builder	None
	1	None	Shorting jumper for 2 place 0.1 inch header pins	None
	1	K1	G6H-2F-DC12 double pole, double throw 12V surface mount relay	G6H-2F-12VDC

Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	4	L1, L2, L3, L4	1m0 RF choke (shielded) high current	None
	1	L5	1m0 RF choke, high current unshielded	5800-102
	2	Q1, Q2	NPN transistors, VHF, type 2N5109	2N5109
	2	None	Heat sinks for Q1 and Q2	None

	2	None	Nylon insulating spacer for Q1 and Q2	None
			¼ watt, 5% carbon film resistors	
	2	R1,R6	560R	Green-blue-brown-gold
	1	R4	51R	Green-brown-black-gold
	2	R10, R5	1K5	Brown-green-red-gold
	4	R2, R7, R9,R11	10R	Brown-black-black-gold
	2	R3, R8	100R Trim-pot	101
	1	RV1	14mm dia. 18V over-voltage MOV	180M
	1	SA1	Spark gap Either of the following may be provided: 90V 75V	90V (and date code) EC 75 (and date code)
Same as J4.	2	TP1, TP2	Test points. Use header pin. May be supplied as a	None

Same as J4	3	None	multiple pin strip to be broken as needed by builder 3 place header pins. May be supplied as a multiple pin strip to be broken as needed by builder	None
	4	T1,T2,T3, T4	0.5 inch diameter ferrite cores; builder to wind	None
	1	PCB	Printed circuit board	
None	1 length #24 wire	None	No. 24 AWG magnet wire, use for T2 and T4	
None	1 length #26 wire	None	No. 26 AWG magnet wire, use for T1 and T3	

Component Layout



Assembly Order

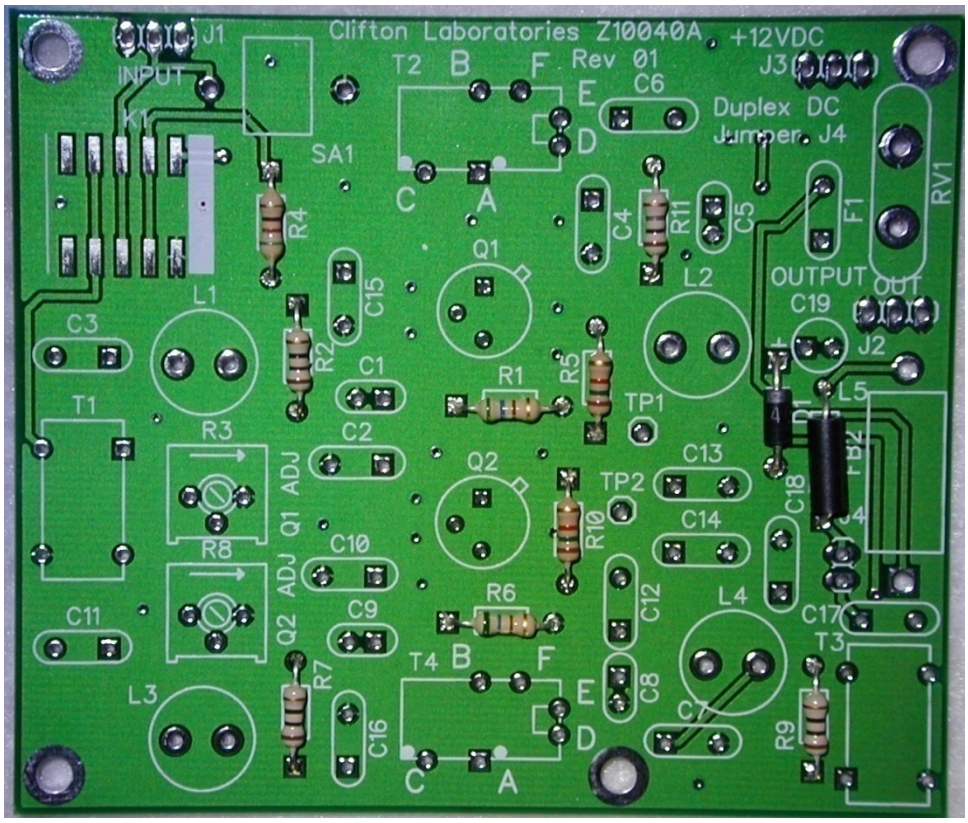
The Z10040A is a relatively simple kit. The most complex part is winding the transformers, and even this is not difficult.

The assembly order generally follows component height—the smallest components are installed first, and the transformers last.

Install the ¼ watt 5% carbon film resistors

- ❑ R1 560R green-blue-brown-gold
- ❑ R6 560R green-blue-brown-gold
- ❑ R4 51R green-brown-black-gold
- ❑ R5 1K5 brown-green-red-gold
- ❑ R10 1K5 brown-green-red-gold
- ❑ R11 10R brown-black-black-gold
- ❑ R9 10R brown-black-black-gold
- ❑ R2 10R brown-black-black-gold
- ❑ R7 10R brown-black-black-gold
- ❑ Install D1, the reverse polarity protection diode. This will be a 1N400x series device, marked 1N400x where x may by any digit from 0 to 7. Observe polarity when installing the diode; the diode body will be marked with a bar or ring around one end. The lead from the marked end goes into the pad marked with a bar and the + sign.
- ❑ Install FB2, the ferrite bead. (FB1 is not used.) The ferrite bead is not marked and is not polarity sensitive.

The photo below shows the PCB at this stage of assembly.



Install 1u0 capacitors (marked 105) at:

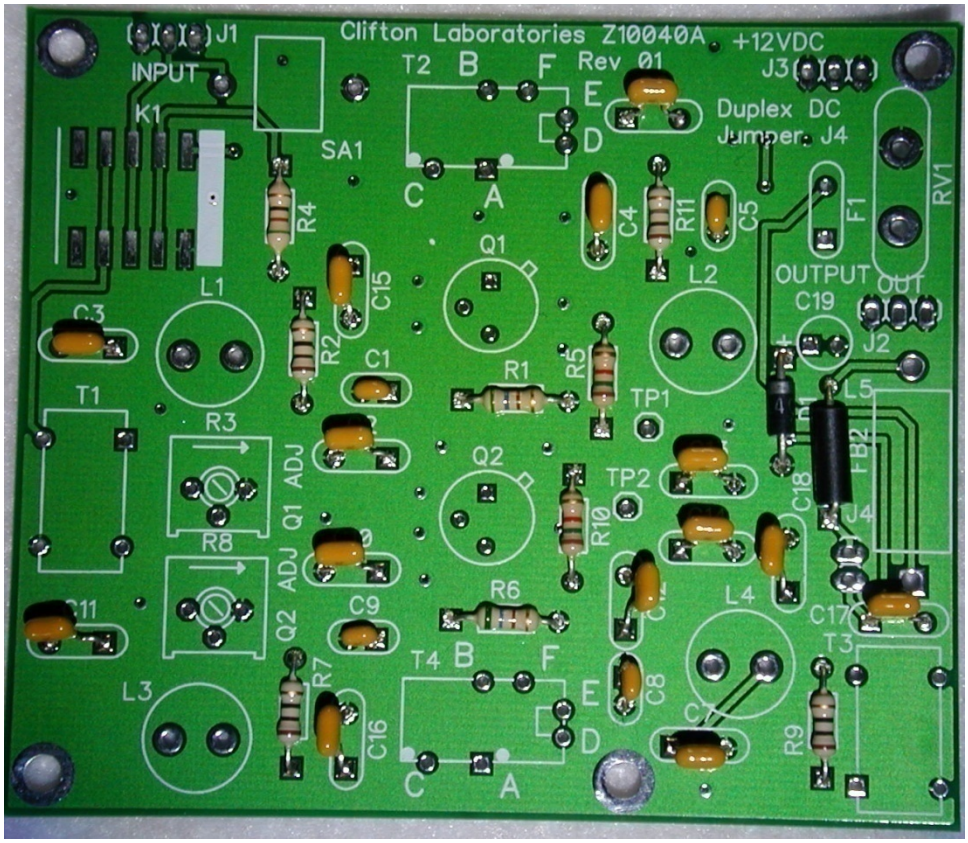
- ❑ C3
- ❑ C11
- ❑ C10
- ❑ C2
- ❑ C4
- ❑ C14
- ❑ C18
- ❑ C17
- ❑ C16
- ❑ C15
- ❑ C6
- ❑ C13

- ❑ C12
- ❑ C7

Install 1000pF capacitors (marked 102 or) at:

- ❑ C1
- ❑ C9
- ❑ C8
- ❑ C5

The photo below shows the PCB at this stage of assembly.



- ❑ Install L5, 1m0 RF choke, marked 5800-102.
- ❑ Install F1 (RXE020 200 mA polyfuse, marked XF020). This component has crimped leads. To install, slip one lead into the mounting hole so that the kink or crimp snaps across the PCB. Put the second lead into the other mounting hole and gently pull (with long nose pliers) the second lead from the underside of the board until it likewise snaps into the mounting hole. If this process is too difficult, you may simply install F1 with the crimped

leads above the PCB surface. Solder.

- ❑ Install RV1, the MOV over-voltage protector, marked 180M. RV1 is not polarized and may be installed in either orientation.

- ❑ Install R3, a 100R trimpot, marked 101.

- ❑ Install R8, a 100R trimpot, marked 101.

Install the four 1m0 shielded RF chokes. Note: the hole spacing is such that the chokes will be slightly above the PCB when installed. These parts are not marked.

- ❑ L1

- ❑ L2

- ❑ L3

- ❑ L4

- ❑ Install C19 (33µF, 63V electrolytic capacitor). This is a polarized part. Polarity may be indicated by either (or both) of the following: (a) The capacitor has a negative side marking; (b) the positive lead is the longest. Install C1 ensuring the positive lead is inserted into the pad marked with the + sign. Solder.

- ❑ Locate the two 2N5109 transistors and the two nylon insulators. Note that the insulator has four notches.



Slip one insulator over each transistor, orienting it so that the three leads fit into notches.

- ❑ Install Q1 (marked 2N5109) with its insulator at Q1. The transistor body / insulator combination should be flush against the PCB surface.

- ❑ Install Q2 (marked 2N5109) with its insulator at Q2. The transistor body / insulator combination should be flush against the PCB surface.

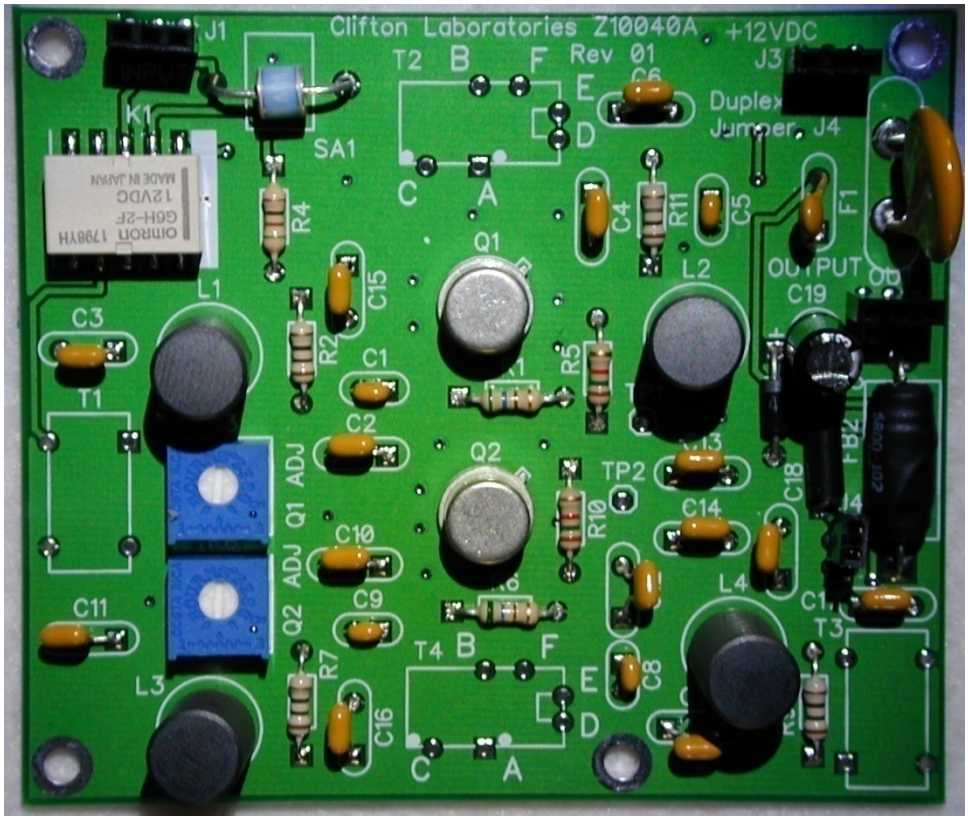
- ❑ Install K1 relay, marked as G6H-2F; orient the marking bar on the relay to match the bar on the PCB outline. To install K1, first apply a light solder coat to one of the end pads on the PCB. Hold K1 on top of the pad and gently press down on it whilst heating the tinned pad. Check K1's alignment to verify that the pins are centered in the associated pad. Solder the diagonal pad. Recheck alignment and solder the remaining pins in place. Touch up the first pad.

- ❑ Install SA1, the spark gap, marked either 90V plus a date code or EC75 plus a date code. SA1 is not polarized and may be installed in either orientation. Be careful when bending the leads as the ceramic body is fragile. SA1 should be installed so that the body is approximately 1/8th inch (3 mm) above the PCB surface.

Install the three-pin header sockets (female) at:

- ❑ J1
- ❑ J2
- ❑ J3
- ❑ Locate the header pin (male) strip and break or cut two pins from the strip. Install the two pins at J4. (The short side goes into the pad holes.)
- ❑ Cut or break two individual pins from the header pin strip.
- ❑ Install one pin at TP1.
- ❑ Install one pin at TP2.

At this point, all components should be installed on the PCB, except for the four transformers and the two heat sinks. The photo below shows the PCB at this stage.

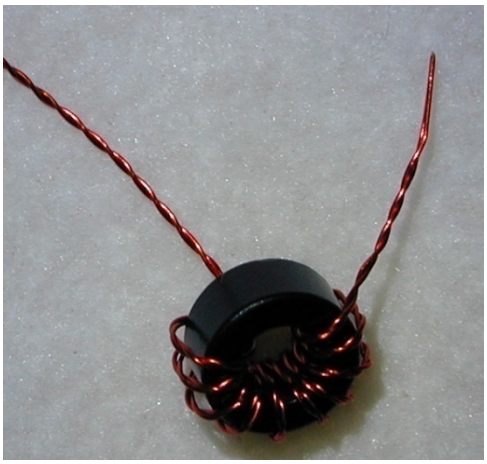


❑ Locate the length of No. 26 AWG magnet wire. (It is the smaller diameter of the two wire lengths.) Cut two lengths, each 22 inches (560 mm) long. Double one wire back upon itself and twist approximately 60 turns. Repeat for the second wire length.



At this point, you should have two twisted wire sections, each approximately 11 inches (280 mm) long, with a loop at one end and two free ends at the other.

❑



Wind the twisted wire 10 turns onto one of the ferrite cores.

As a reminder, a turn is counted when the wire passes through the hole in the core.

Start by inserting the cut end approximately one inch (25 mm) through the core. Thread the doubled end through and wind 10 turns. Space the turns so that the windings occupy approximately 75% of the core perimeter (270 degrees if you prefer to think in those terms).

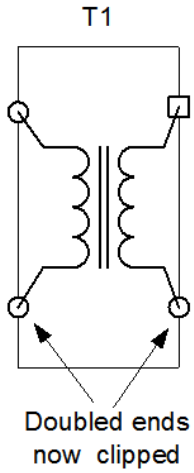
Repeat for the second transformer.

Congratulations. You have completed winding two bifilar broadband transformers, T1 and T3.

Locate the PCB and look at the outline for T1 and T3. Note that each has four pads, comprised of three round pads and one square pad, oriented as shown in the drawing.

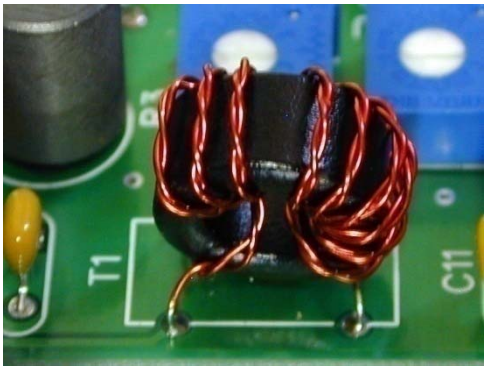
The leads that are now doubled together install in the two bottom round holes. (Either lead can go in either hole.)

Cut the doubled end of one transformer so that approximately one inch (25mm) extends beyond the core. Keep track of which leads were formerly doubled. Un-twist the pigtails so that you have four separated wires. Remove the insulation and tin the four wires. Using an ohmmeter, identify the ending wire associated with each of the two doubled wires and install the transformer as shown in the drawing at T1.



❑ Repeat this process for T3 and install.

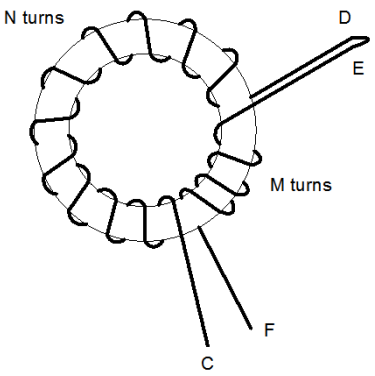
Your transformers should resemble the one photographed at the right.



❑ The remaining step is to wind T2 and T4, the matching and feedback transformers. These transformers should be as identical as possible and must be phased (wound) the same way or else you will build an oscillator instead of an amplifier. If you carefully follow the instructions in this manual, your transformers will work the first time. Before winding T2 and T4, take a moment to read the installation steps and study the drawing and photographs.

This manual describes transformers resulting in 11 dB nominal gain, with a 1:11:4 winding ratio. Other winding ratios are possible with different gain as described elsewhere in this manual. In the context of drawing below, this configuration is N=11, M=4.

❑ Cut two lengths of #24 AWG magnet wire, each length 16 inches (400 mm) long.



This wire will be wound 15 turns on a ferrite core, as illustrated at the right. The letters C…F on the drawing correspond to T2 and T4's PCB pads.

Before winding the transformers, take a moment and look at the PCB outline for T2 and T4.

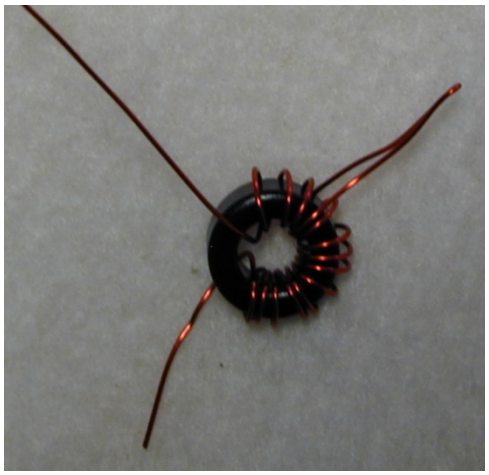
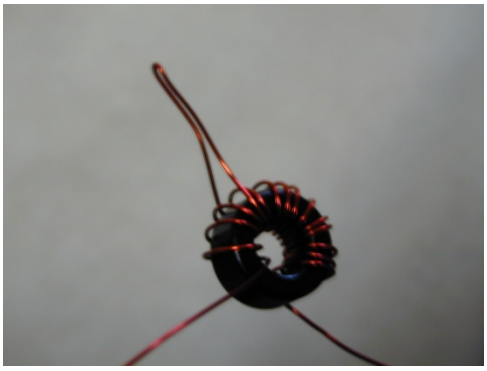
Start by threading the wire through the core with approximately one inch (25 mm) projecting from the core. This short end is C in the drawing.

Wind 11 turns (N) following the orientation shown in the drawing. Note the direction of winding. (I'm left handed and this is how I wind toroids.) When completed with all 15 turns, the winding will occupy 80 to 85% of the core perimeter.

As a reminder, a turn is counted when the wire passes through the hole in the core.

Extend the 11th turn approximately one inch (25 mm) and double it back. (The doubled wire will become ends D and E). Wind four more turns (M), ending at end F. Trim the F wire to be approximately one inch (25 mm) long.

The photos below shows a transformer at this stage, before the loop is cut and the end wires trimmed.

❑  

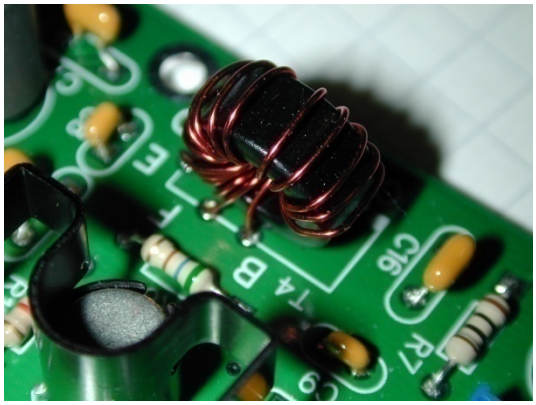
❑ Cut the loop so that the two free ends are approximately one inch (25 mm) long. Remove the insulation on all four ends and tin. You may find it helpful to fit the transformer into the PCB to see how it fits before continuing to the next step.

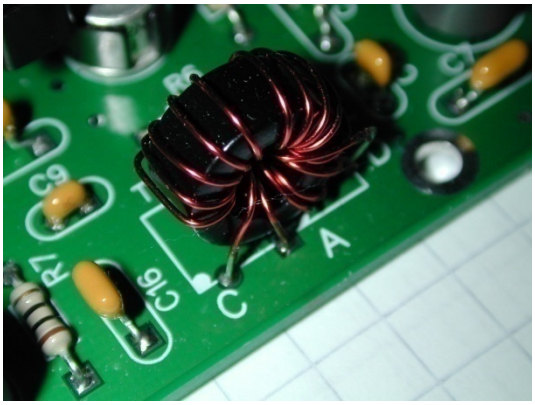
❑ Insert the leads into T2 holes C, D, E and F, following the drawing, and solder these four leads.

❑ Locate the remaining length of No. 24 AWG magnet wire and cut two lengths 1.25 inch (32 mm) long. These will be the single turn winding A-B. Strip and tin each end approximately 0.25 to 0.375 inches (6.5 mm to 9.5 mm) and install between pads A and B, passing the wire through the transformer's central hole. Installing this wire will be easier if you install the wire vertically (not passed through the core) in the pad away from the board edge. Solder the wire in place. Then pass it through the transformer core and into the outside pad hole. Solder.

❑ Repeat this process for T4 with the second transformer.

The photographs below show T4 installed.





❑ Install the heat sinks on Q1 and Q2. If you have it, a small amount of heat sink compound or thermal grease can be used to improve the thermal connectivity between the heat sink and the transistor body.

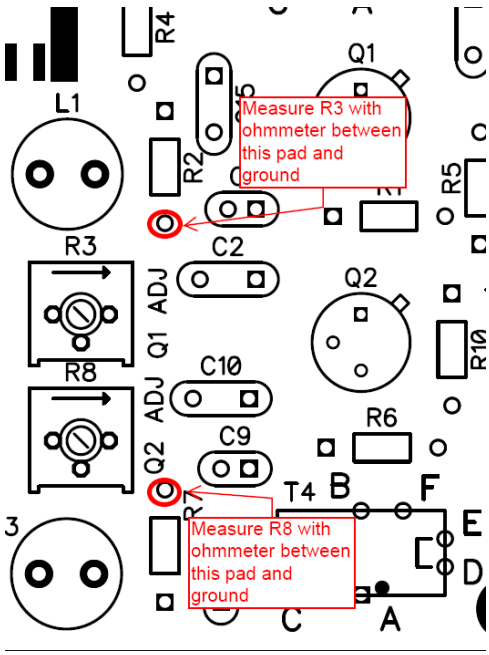
Post Construction Adjustment and Checkout

Before powering up the Z10040A, take a moment to make resistance checks and pre-set R3 and R8.

❑ With an ohmmeter measure and adjust R3 and R8 to 50 ± 2 ohms. (Both measuring points are with respect to ground, with the negative lead of the ohmmeter to ground.)

R3: Measuring point is junction of R3 and R2, as illustrated to the right.

R8: Measuring point is junction of R8 and R7 as illustrated to the right.



You may wish to make a complete set of resistance measurements as developed in the maintenance section of this manual, or you may wish to make an abbreviated set of resistance measurements described below before apply power for the first time.

All readings are taken with a Fluke 189 digital multimeter with low-voltage ohms. Negative lead to ground and positive lead to the indicated test point. Look for gross divergence from these values, not small differences, as different ohmmeters may yield different results where semiconductor junctions are in the path. Since the Z10040A has two identical sections comprising the push-pull design, look for differences in symmetry, where the equivalent point reads significantly different in one section compared with the other.

❑

Abbreviated Resistance Checks Before Applying Power		
Test Point	**Value (Ohms)**	**Comment**
TP1	510	
TP2	510	
Q1 collector	520	Q1's case is internally connected to the collector.
Q2 collector	520	Q2's case is internally connected to the collector.
DC Input (J3) center	510	Should be the same with and without a jumper at J4

❑ If you have not already done so, make up a power cable using a three-pin male header pin. Positive to the center pin and negative to the two outside pins.

❑ The Z10040A will work with DC supply voltages up to 15V and down to 12V. Performance data is based upon 13.8V DC and in general slightly improved intermodulation performance will be seen with supply voltages between 13.8 and 15.0V.



If a laboratory power supply with current limiting is available, set it for a maximum short circuit current of 175 mA and set the voltage to 0V. Connect the supply to the Z10040A at J3 (J4 duplex jumper open) and bring up the voltage slowly whilst observing the current. With R3 and R8 set for 50 ohms, the maximum current observed should be approximately 100 mA at 13.8V. If significant deviations from this value are observed, immediately remove power and investigate.

Adjusting R3 and R8. With the normal DC supply voltage applied through J3 (J4 duplex jumper open) preferably with a laboratory power supply with current limiting set to 175 mA, adjust R3 and R8.



Note: If you adjust R3 or R8 to the zero ohms extreme, it may be possible to damage components in the Z10040A. Some current limiting is built into the circuit, via R2 and R7, together with the resistance of L1 and L3. However, in order to provide the maximum adjustment range to compensate for variations in Q1 and Q2, complete protection against mis-adjustment is not possible. Accordingly, when adjusting R3 and/or R8, it is imperative that you observe the total current being drawn by the amplifier, and, if possible, use a power supply with current limiting set to 175 mA.

In particular, the 1mH shielded inductors used at L1, L2, L3 and L4 are rated for a maximum DC current of 90 mA. Under no circumstances should Q1 or Q2 be biased to draw more than 75 mA each.

❑ Alternative 1: If you do not have the ability to measure 3rd order and 2nd order intermodulation products, adjust R3 and R8 such that Q1 and Q2 have substantially equal collector currents of approximately 45 mA each.

Collector current is determined by measuring the voltage drop across the 10R resistors, R11 and R9 via TP1 and TP2. The drop across R9 and R11 represents the sum of the collector current and the current drawn by the base bias network, which is approximately 6 mA.

Connect a DC voltmeter between the junction of F1/RV1 (positive lead) and TP1 (negative lead.) Adjust R3 until the voltmeter reads 0.500 ±0.050 volts. This corresponds to 50 mA total current , or approximately 44 mA collector current through Q1 and 6 mA bias network current. Record the DC voltage: _____

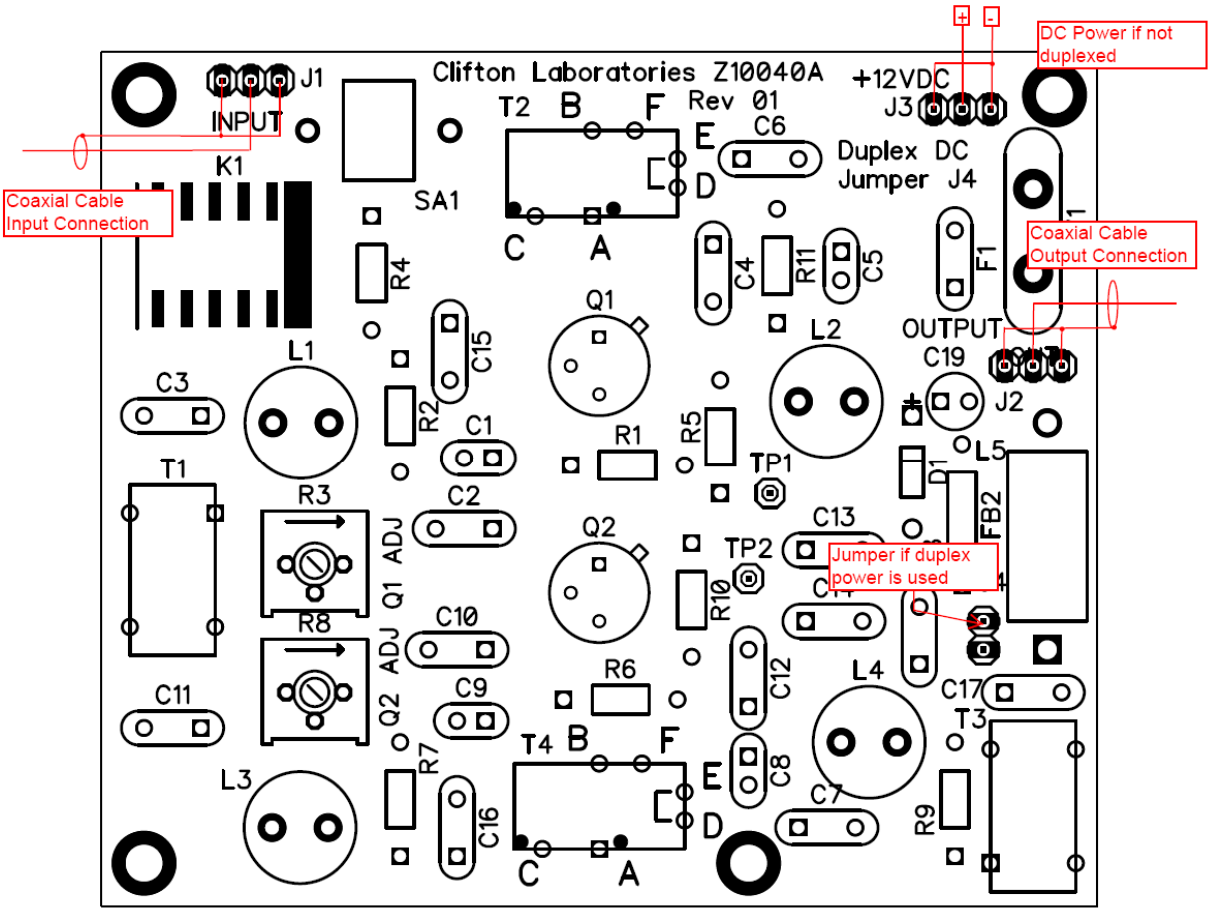
Move the negative lead to TP2 and adjust R8 for the same reading recorded above. This will set Q2's collector current to approximately match Q1's current.

❑ Alternative 2: Adjust R3 and R8 for best 3rd and 2nd order intermodulation performance using the test equipment configuration you normally use for these measurements. During the adjustment process do not exceed 75 mA in either Q1 or Q2 as it is possible to damage components with over-current.

A bias adjustment service for kit builders not equipped to measure IP2 and IP3 is available. Contact Clifton Laboratories for details.

Input, output and DC power connections are made to the Z10040A with 3-pin headers. Since the outside pins are always ground, either orientation is permitted.

As always when making connections to a high gain amplifier, shielded coaxial cable should be used and the output cable should not be routed near the input and vice versa.



This completes the assembly and verification of your Z10040A Norton Amplifier.

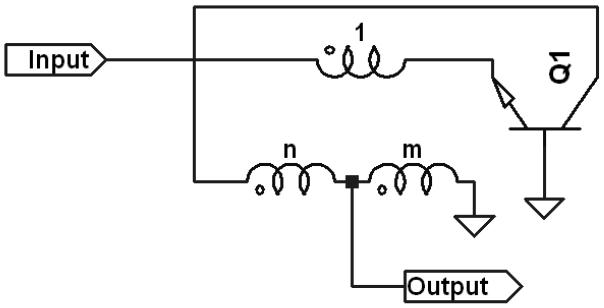
Schematic and Theory of Operation

Theory of Operation

The Z10040A Norton amplifier consists of two identical amplifier sections arranged in push-pull.

The discussion below uses component designations for the section associated with Q1.

Each section is a common base (also known as "grounded base") amplifier. As such, essentially identical signal currents flow through all three sections of T2 and T1's secondary winding. Gain is achieved in the grounded base amplifier because the collector load, represented by T2's n and m windings operating as an auto-transformer has greater impedance than the emitter input, and hence power gain results.



The figure at the right is a simplified view of an amplifier section, with all DC biasing and blocking components removed so that we may concentrate on the signal flow. The transformer turns ratios are shown as 1:n:m, but this does not mean the emitter feedback winding must have only one turn. Rather, it is the ratio of turns that is important, so that if the emitter winding has, for example, two turns, then the number of turns in windings n and m should also be doubled.

Consider windings n and m and assume a load of impedance Z is connected from output to ground. Windings n and m form an auto-transformer with Q1's collector seeing an impedance of:

$$Z_C = Z_O\left(\frac{n+m}{m}\right)^2$$

Since the same signal current flows through the emitter and collector (neglecting base current), the gain of the common base amplifier is proportional Zc or n and m in this relationship.

The transformer turns ratios should not be arbitrarily selected, if the full benefits of the Norton amplifier are to be realized. From Patent No. 3,891,934, the following equation governs the transformer turns relationship:

$$n = m^2\left(\frac{R_S}{R_L}\right) - m - 1$$

$$n = m^2 \left(\frac{R_S}{R_L}\right) - m - 1$$

Where

R_S is the source (input) impedance

R_L is the load (output) impedance

n and m are the transformer winding ratios, normalized to an emitter winding with one turn.

In our case, we wish the input and output impedances to be equal, and hence $R_S/R_L = 1$. Thus the turns relationship is simplified to:

$n = m^2\text{-}m\text{-}1$

The amplifier's transducer gain[1] is stated as:

$$G_t = m^2 \frac{R_S}{R_L}$$

Again, since our normal operation is with equal input and output impedances, the transducer gain G_t is simply m^2.

Winding Ratio 1:n:m	Transducer Gain (dB)
1:1:2	6.0
1:5:3	9.5
1:11:4	12.0
1:19:5	14.0

These figures are theoretical and the actual realizable gain is typically a dB or so less.

One significant advantage of the Norton amplifier is that the input impedance automatically tracks the output impedance. Thus, if terminated into a 50 ohm load, the input impedance is 50 ohms. If the output impedance is changed to 75 ohms, the input impedance becomes 75 ohms. (This relationship is again not perfect, but it is reasonably good with less than a 2:1 VSWR over the range 300 KHz – 30 MHz when measured in a 50 ohm system.)

DC power may be provided to the Z10040A via two feed points. First, a three-pin connector permits direct DC power connection. Secondly, adding a jumper at connector J4 permits DC power to be duplex fed over the coaxial cable transmission line carrying the amplifier's output. Of course, an appropriate DC power injector, such as Clifton Laboratories model Z1202A, will be required and the power source that is used should be selected to have low noise at the frequencies of interest.

1 Transducer gain is defined as: "the ratio of the power delivered by a network to a load (PdL) to the power available from the source (Pas). Transducer gain is a function of the source and load reflection coefficients and the network s-parameters." http://www.maurymw.com/support/faqs/faqs/faq9.html

Over current protection is provided by F1, a 200 mA positive temperature coefficient "polyfuse." Should the amplifier draw more than 200 mA, F1 will heat and switch to a high resistance state, thereby limiting the current drawn by the power source. So long as the voltage remains applied, F1 will remain in the high resistance state.

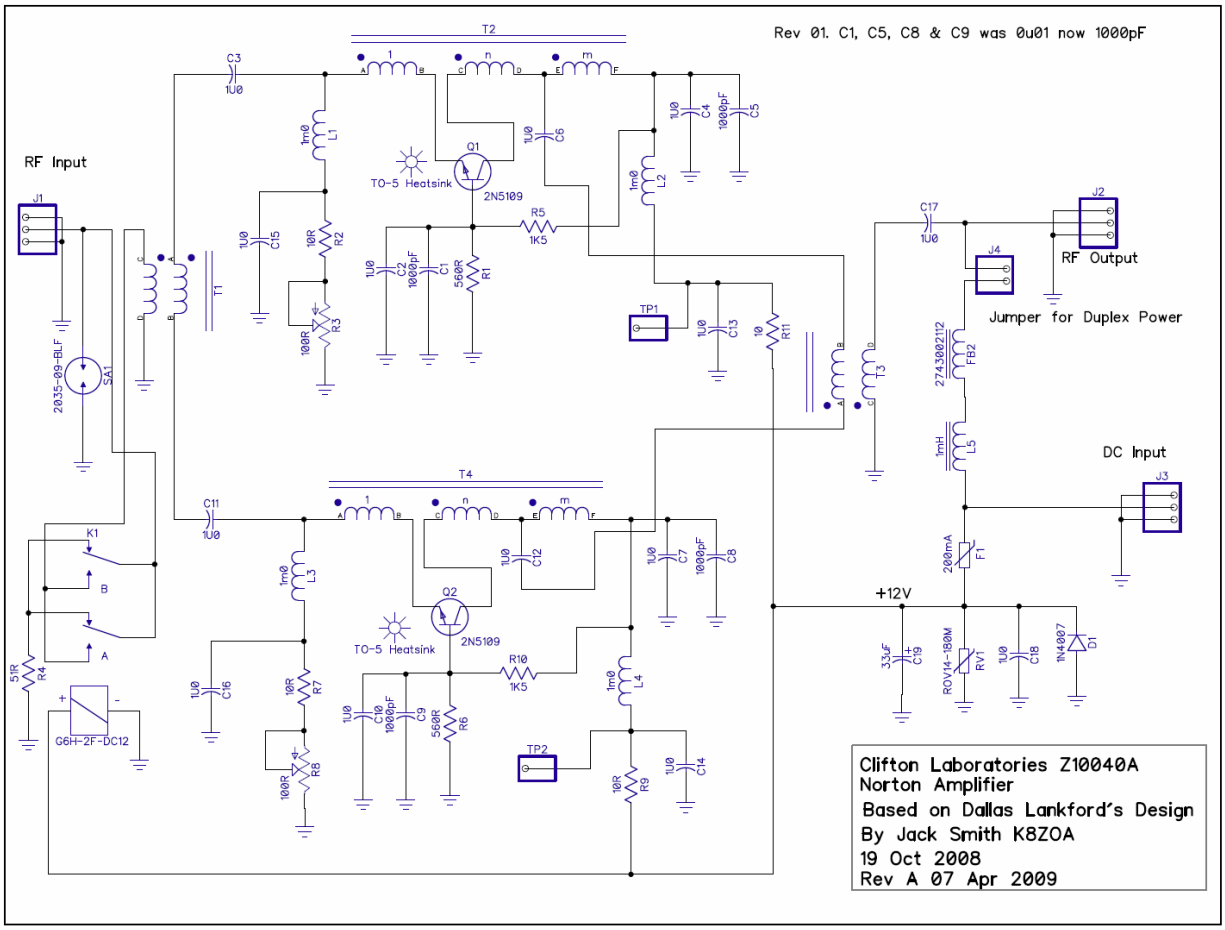
Over voltage protection is provided by RV1, an 18V DC (nominal) bipolar metal oxide varistor. The primary purpose of RV1 is to limit damage to the DC power source, should a nearby lightning strike or other incident induce a greater than normal voltage on the DC power line. Although RV1 is rated to begin clamping at 18V (1.0 mA clamp current at 18V), the actual onset voltage may be 20% above this figure and the clamping voltage may rise as high as 36V at 50A clamping current. Hence, even with RV1 in place and functioning properly, excessive over voltage may still occur if the disturbing event is sufficiently energetic. (The ROV14-180M device used in the Z10040A is rated at a one-time 1,000A clamp or two-times 500A clamp. However, at 1000A, the expected clamping voltage is 80V.)

Reverse voltage protection is provided by D1, a 1N400x series diode connected to be forward biased if the input polarity reverses. This causes two things to happen. First, the maximum voltage across the DC power distribution circuitry will be limited to approximately 1V by D1. Secondly, fuse F1 will enter into high resistance mode by virtue of the over current. Of course, a sufficiently robust power supply connected with reverse polarity may destroy D1 before F1 can enter high resistance mode.

The Z10040A's input circuit is protected in two ways. First, when DC power is removed from the Z10040A, relay K1 removes the input connection and connects it to ground through R4, a 51 ohm resistor. (If desired, the user may replace R4 with a jumper to ground the input when power is removed.) Secondly, SA1, a "gas trap" or spark protector is always connected across the Z10040A's input connector. SA1 limits the voltage although for fast rise time pulses, the break over voltage may be several hundred volts. The primary purpose of SA1 is to limit the voltage that might otherwise be coupled over the coaxial transmission line and, secondarily, to provide some protection to the Z10040's components.



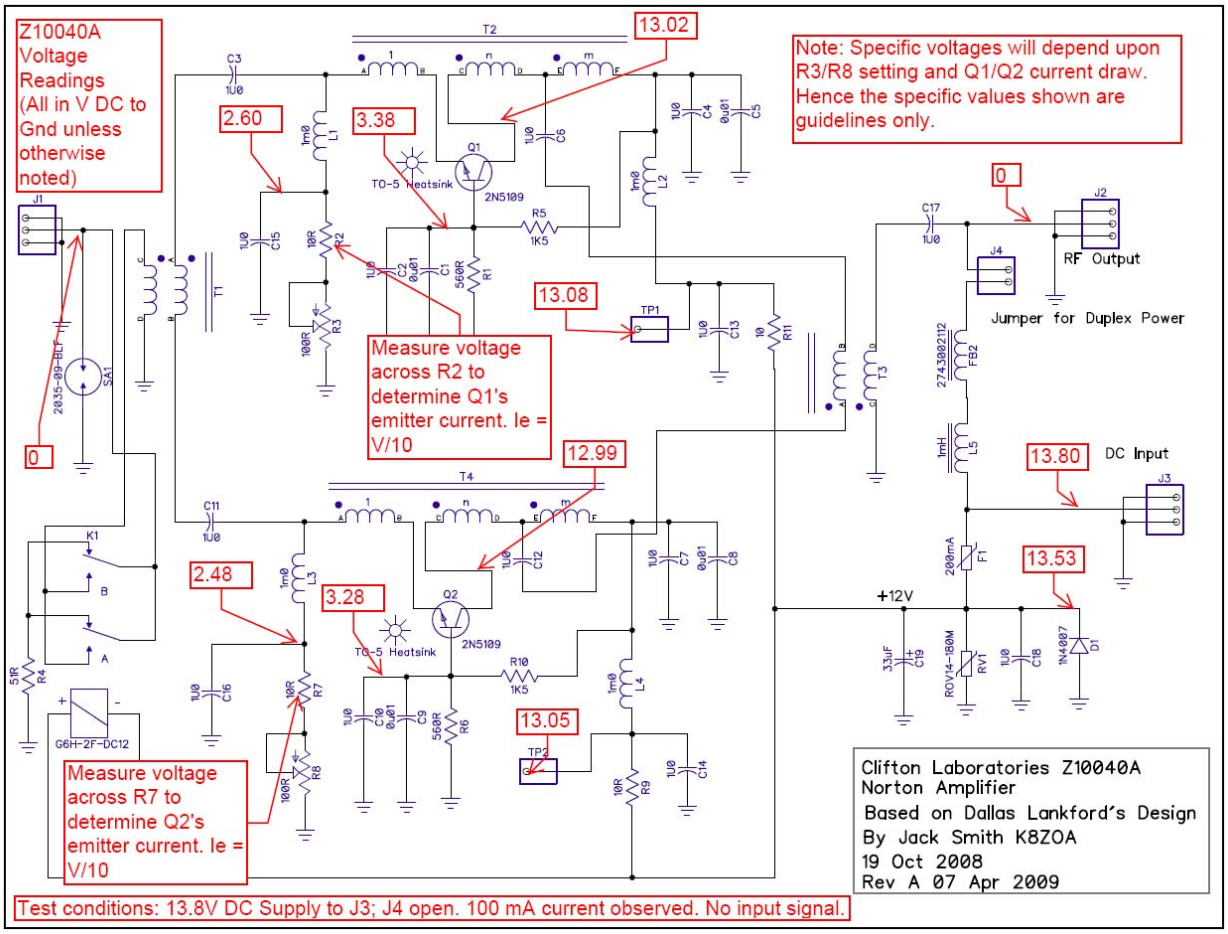
All of these protection measures assume that the Z10040A is properly grounded and that good engineering practices have been used in its installation and construction of the ground system. The Z10040A is not intended to survive a direct lightning strike to an antenna connected to its input, whether powered up or not. However, the protective measures incorporated into the Z10040A's design should aid in reducing damage, particularly where the strike is not directly to the antenna system.


Rev 01. C1, C5, C8 & C9 was 0u01 now 1000pF
RF Input
RF Output
Jumper for Duplex Power
DC Input
+12V
TO-5 Heatsink
2N5109
TO-5 Heatsink
2N5109
G6H-2F-DC12
2035-09-BLF
Clifton Laboratories Z10040A
Norton Amplifier
Based on Dallas Lankford's Design
By Jack Smith K8ZOA
19 Oct 2008
Rev A 07 Apr 2009

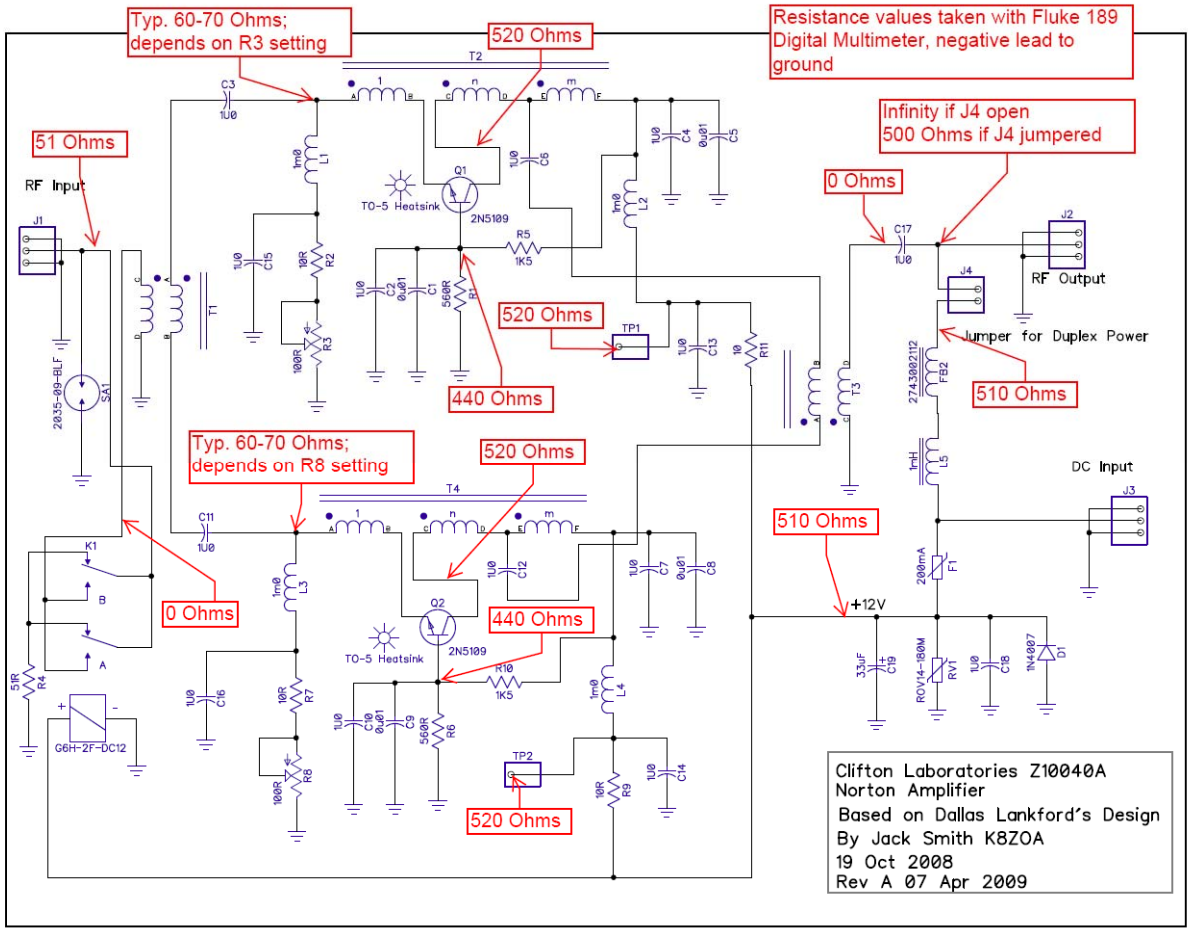
Troubleshooting Guide

The following annotated schematics provide resistance and typical operating voltage data for the Z10040A.

Voltage Data



Resistance Data

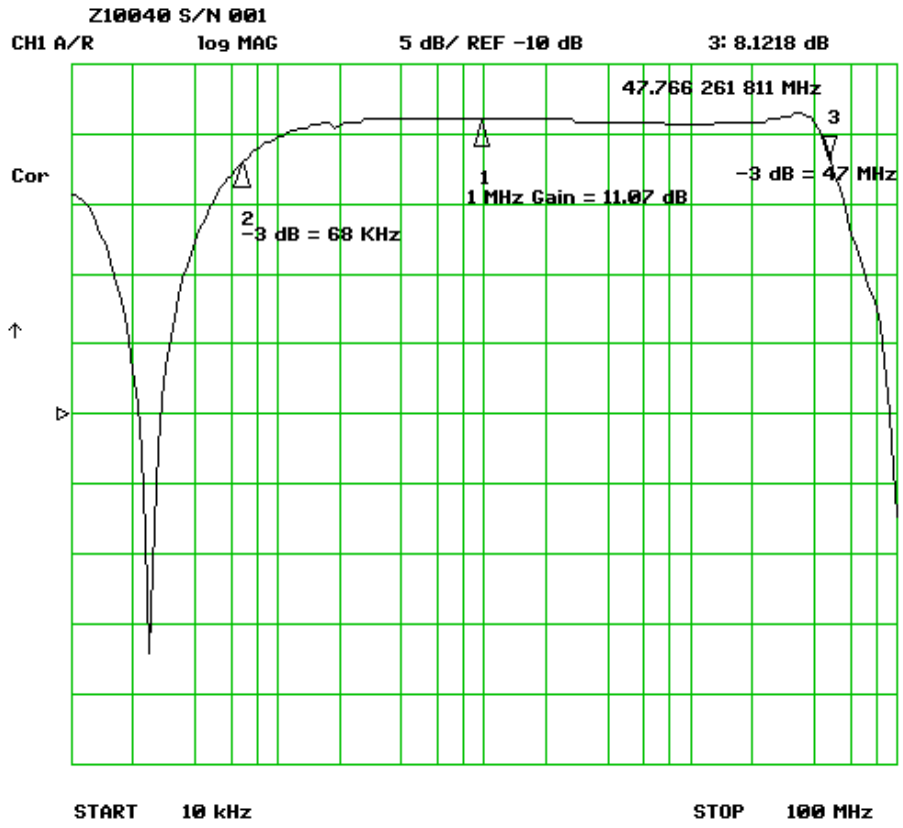


Appendix A Typical Performance Data

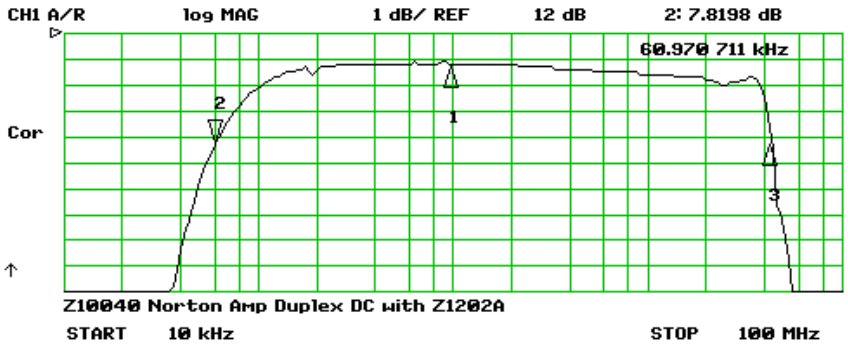
The data presented below is taken from one Z10040A amplifier. While it is believed representative of the Z10040A amplifier, due to component tolerance, assembly practices and test setup, the performance level seen in these measurements should be regarded as *typical* and is not guaranteed.

Bandwidth

Test Conditions: Direct DC feed.



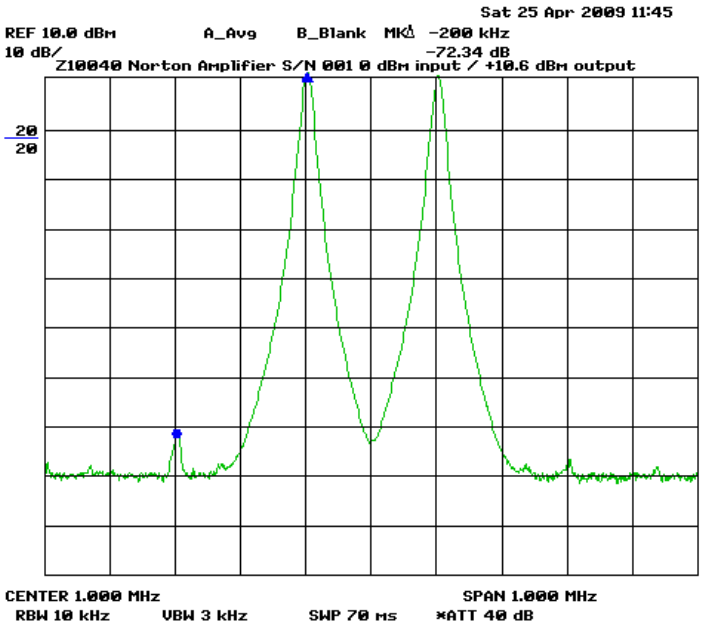
Test Conditions: Duplex DC feed over coaxial cable with Clifton Laboratories Z1202A power coupler.



N	STIMULUS	val
1	1 MHz	10.832 dB
2	60.970 711 kHz	7.8198 dB
3	43.064 683 001 MHz	7.8390 dB

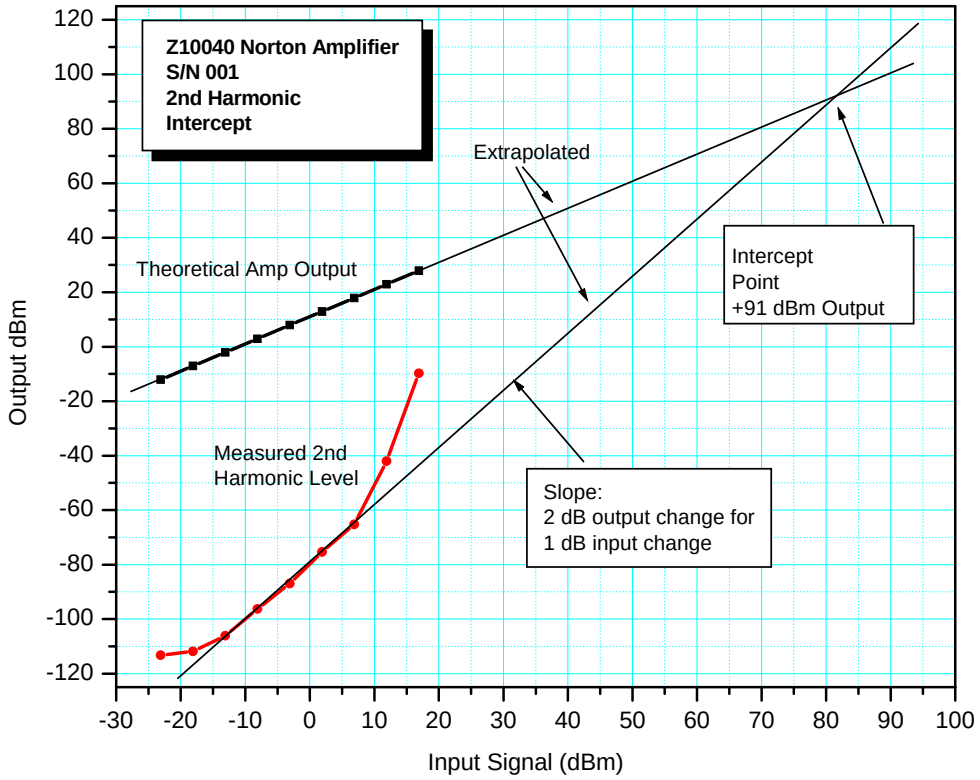
Third Order Intermodulation

Test conditions: Two test signals at 900 KHz and 1100 KHz at 0 dBm (each tone).



Second Harmonic

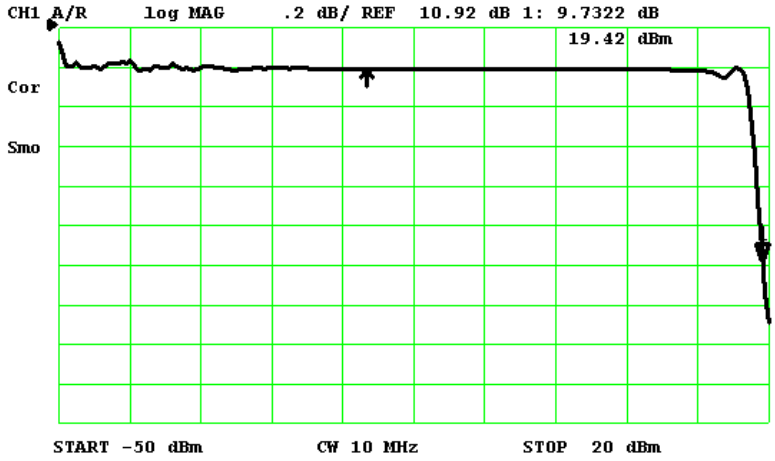
Test Conditions: 5.4 MHz



1 dB Gain Compression

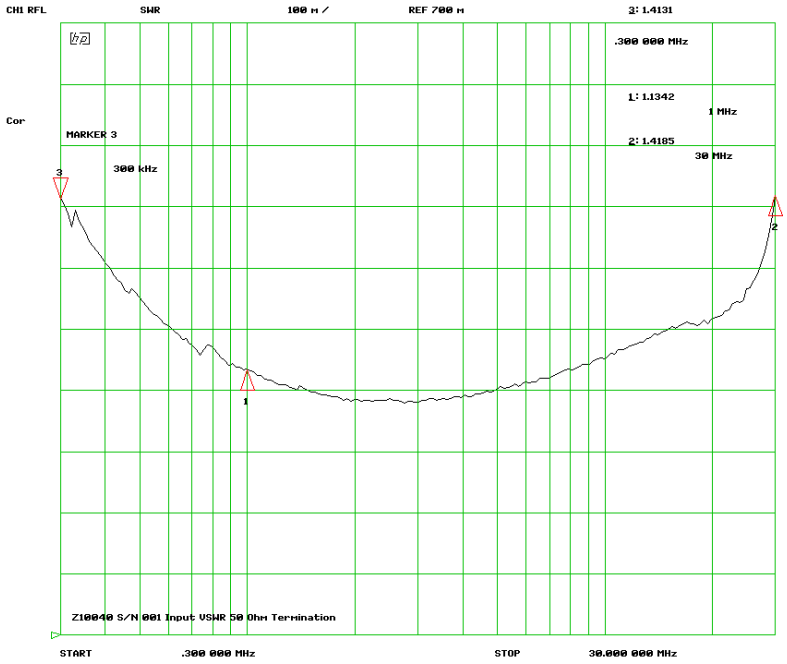
Test Conditions: CW signal at 10 MHz, Z10040A input level between -50 dBm and +20 dBm. 1 dB gain compression point +19.42 dBm input.

Note: This test can easily damage test equipment as the output power approaches 1 watt. Appropriate attenuators must be used to limit signal levels to safe values.



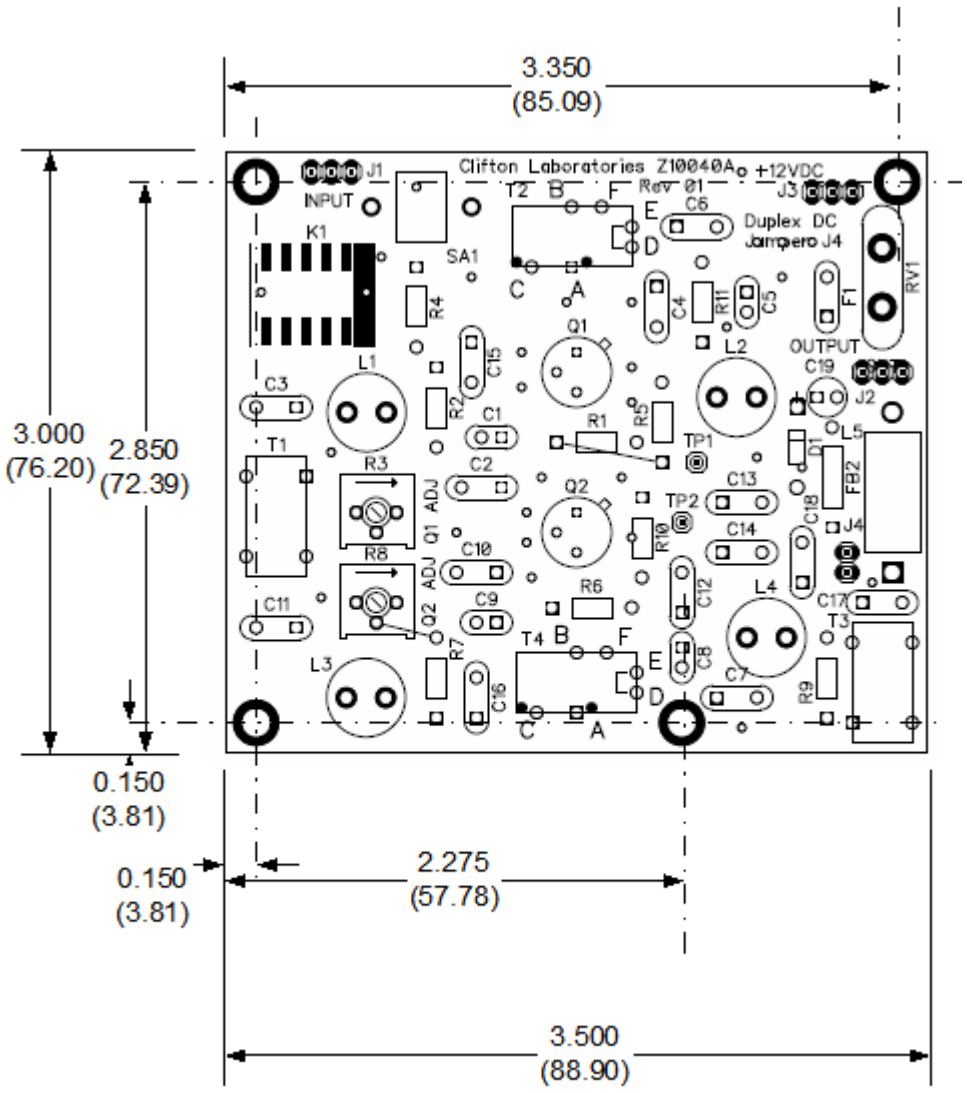
Input VSWR

Test conditions: Terminated with 50 ohm load, 13.8V DC power.



Appendix B – PCB Mounting Hole Dimensions

Drawing is **not** to scale.



Dimensions in inches and (mm)

Appendix C – Norton Amplifier Patent, US Patent No. 3,891,934

United States Patent [19]

Norton et al.

[11] **3,891,934**

[45] **June 24, 1975**

[54] **TRANSISTOR AMPLIFIER WITH IMPEDANCE MATCHING TRANSFORMER**

[75] Inventors: **David E. Norton**, Framingham, Mass.; **Allen F. Podell**, Los Altos, Calif.

[73] Assignee: **Adams-Russell Co., Inc.**, Waltham, Mass.

[22] Filed: **May 22, 1974**

[21] Appl. No.: **472,281**

[52] **U.S. Cl.** **330/21**; 330/19; 330/26; 330/165; 330/188; 330/195

[51] **Int. Cl.** **H03f 3/04**

[58] **Field of Search** 330/12, 19, 21, 22, 40, 330/165, 188, 195

[56] **References Cited**

UNITED STATES PATENTS

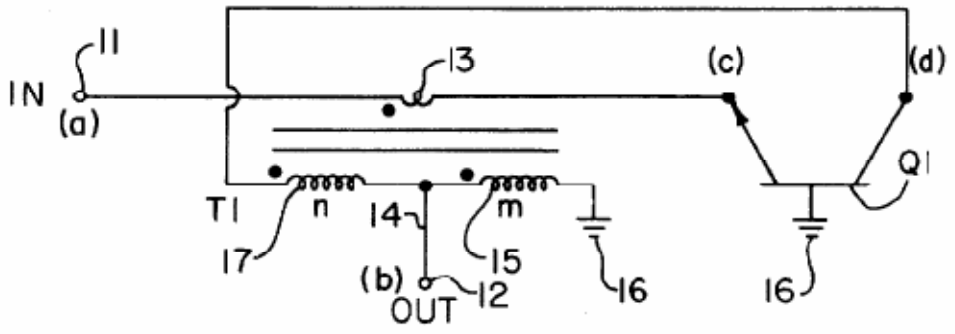
2,691,077	10/1954	Korns	330/40 X
2,701,281	2/1955	DeWhite et al.	330/12 X

Primary Examiner—R. V. Rolinec
Assistant Examiner—Lawrence J. Dahl
Attorney, Agent, or Firm—Charles Hieken, Esq.; Jerry Cohen, Esq.

[57] **ABSTRACT**

An amplifier includes a transistor and transformer having a primary winding and a tapped secondary winding. The primary winding is connected in series between the input terminal and the transistor emitter. The transistor base and one end of the secondary winding is grounded. The other end of the secondary winding is connected to the transistor collector. The transformer secondary tap is connected to an output terminal. The ratio of that portion of the secondary turns connected between the tap and *r-f* ground and the primary turns is m. The ratio of that portion of the secondary turns connected between the tap and the transistor collector and the primary turns is n. For two-way impedance match between a source resistance R_s and a load resistance R_L, $n = m^2 (R_s/R_L) - m - 1$.

8 Claims, 5 Drawing Figures



1

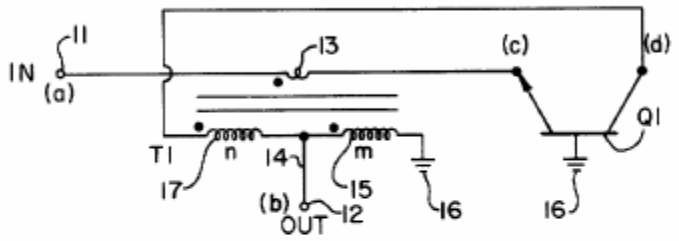


FIG. 1

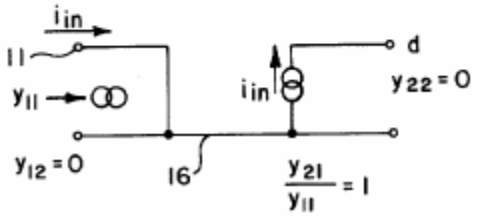


FIG. 2

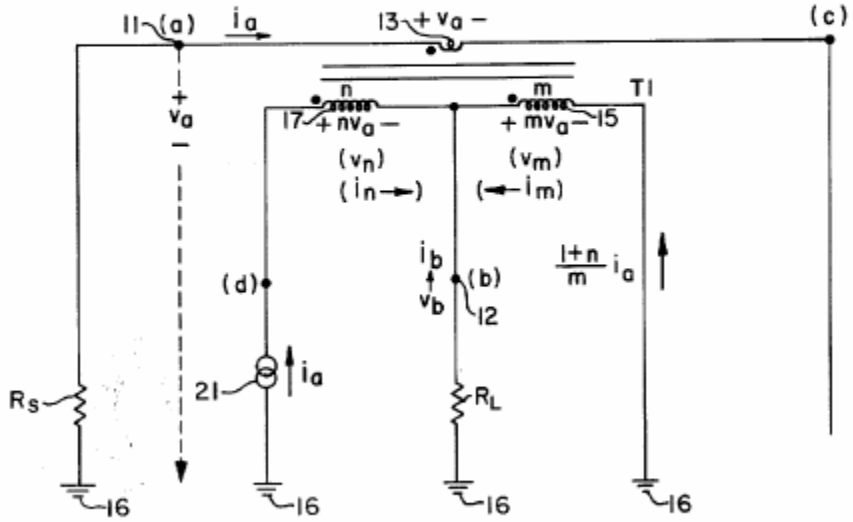


FIG. 3

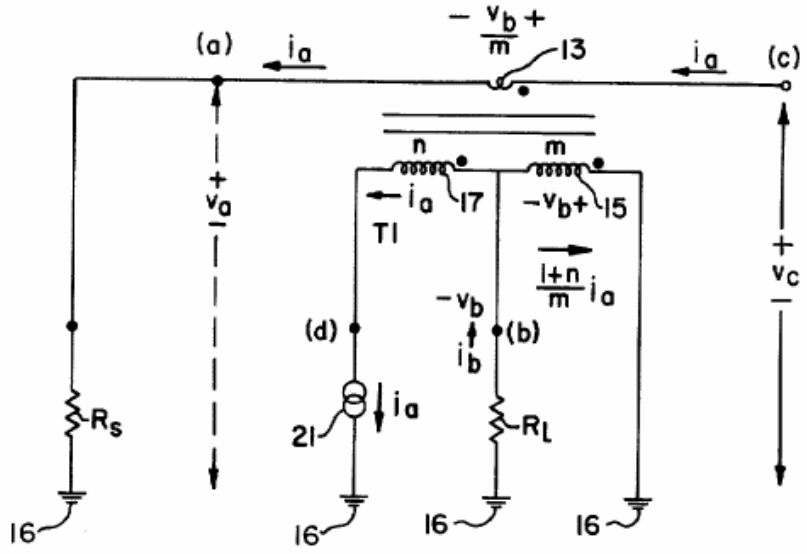

(a)
i_a
$-\frac{v_b}{m}+$
13
i_a
(c)
n
m
$+v_a-$
i_a
17
$-v_b+$
15
T1
$+v_c-$
$\frac{l+n}{m} i_a$
$-v_b$
(d)
(b)
i_b
i_a
21
R_s
R_L
16
16
16
16

FIG. 4

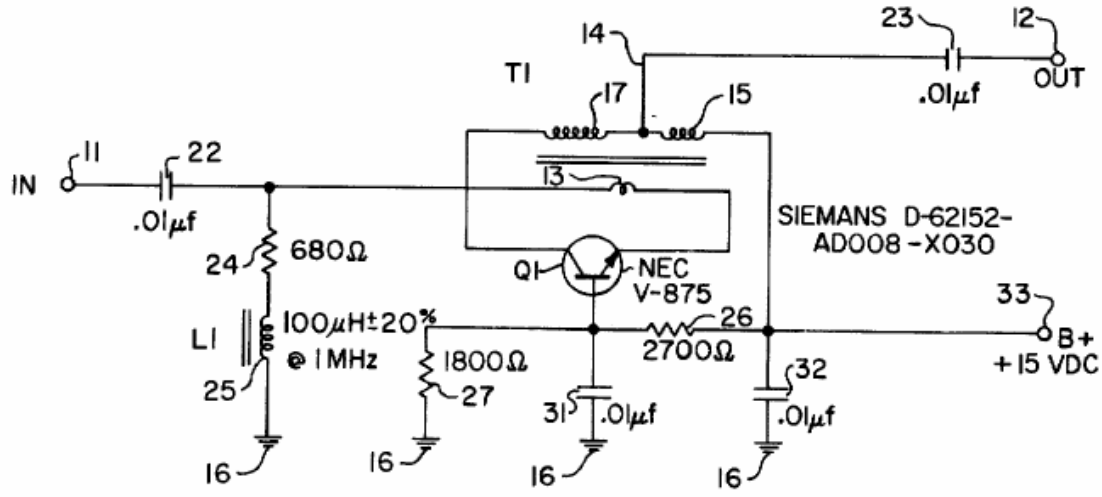

14
23
12
T1
17
15
.01μf
OUT
IN
11
22
13
.01μf
SIEMANS D-62152-
AD008-X030
24
680Ω
Q1
NEC
V-875
33
L1
100μH±20%
@ 1MHz
26
2700Ω
B+
+15 VDC
1800Ω
27
31
.01μf
32
.01μf
25
16
16
16
16

FIG. 5

TRANSISTOR AMPLIFIER WITH IMPEDANCE MATCHING TRANSFORMER

BACKGROUND OF THE INVENTION

The present invention relates in general to ampifying and more particularly concerns a novel amplifier with high dynamic range and efficiency especially useful in matching both a source impedance and a load impedance while providing *r-f* amplification over a relatively broad band with a single transformer and single transistor.

CATV coaxial cable systems that transmit and amplify television signals use many amplifiers representing a significant cost of the system. To avoid reflections that cause undesirable visible ghosts on a television screen, care is taken to properly terminate the transmission lines. Thus, both the input and output of an amplifier should match that of the transmission line to which it is connected. While techniques for achieving this result are known, conventional prior art circuits involve many components that are relatively costly to acheive this result.

Still another problem arises from the range of signal levels to be amplified. It is difficult to amplify low level signals adequately and avoid overloading the amplifier with high level signals. Furthermore, dissipation of *r-f* power in amplifying circuit resistors reduces efficiency.

Accordingly, it is an important object of this invention to provide an economical low-noise *r-f* amplifier with high dynamic range and efficiency capable of conveniently matching both a source impedance and a load impedance while providing good amplification over a relatively broad bandwidth.

It is another object of the invention to achieve the preceding object with relatively few components.

It is a further object of the invention to achieve one or more of the preceding objects with relatively few components, none of which need be adjusted once circuit design is complete.

It is still a further object of the invention to achieve one or more of the preceding objects with a circuit that has only one transistor and one transformer.

SUMMARY OF THE INVENTION

According to the invention, there is an amplifying device having control, input and output electrodes, such as a transistor having at least base, emitter and collector electrodes. Means are provided for effectively connecting at *r-f* the control electrode or base to a common or reference terminal. Transformer means having at least a primary winding and a tapped secondary winding has the primary winding coupled in series between an input terminal and the input electrode or emitter and its secondary winding effectively coupled between the common terminal and the transistor collector. An output terminal is coupled to a tap between first and second portions of the transformer secondary winding, the first portion being coupled between the tap and the common terminal. The ratio of first portion turns to primary turns is m; of second portion turns to primary turns, *n*. Preferably $n = m^2(R_s/R_L) - m - 1$ where R_s and R_L are the source and load resistances to be matched at the input and output terminals, respectively.

Numerous other features, objects and advantages of the invention will become apparent from the following

specification when read in connection with the accompanying drawing in which:

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a schematic circuit diagram of an embodiment of the invention;

FIG. **2** is a representation of the transistor as an ideal common base circuit with various admittance parameters;

FIG. **3** is an equivalent circuit of the circuit of FIG. **1** helpful in understanding the mode of operation;

FIG. **4** is the circuit of FIG. **3** redrawn to help determine the source impedance presented to the emitter; and

FIG. **5** is a schematic circuit diagram of a preferred embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

With reference now to the drawing and more particularly FIG. 1 thereof, there is shown a schematic circuit diagram of an embodiment of the invention for providing gain between input terminal **11** and output terminal **12** while matching a source impedance R_s connected to input terminal **11** and a load impedance R_L connected to output terminal **12**. The circuit comprises transistors Q1 and transformer T1. So as not to obscure the principles of the invention the specific means for applying operating and biasing potentials to the particular circuit elements are not shown, those skilled in the art knowing how to supply these potentials. For example, the collector may recieve d-c operating potential through the secondary winding of transformer T1 from a d-c supply bypassed to ground by a suitable capacitor in a manner well-known in the art.

For convenience in the explanation which follows below input terminal **11**, output terminal **12**, the emitter and the collector are designated nodes *a*, *b*, *c* and *d*, respectively. The primary winding **13** is connected between input terminal **11** and the emitter. The secondary winding of transformer T1 has a tap **14** connected to output terminal **12** and a first portion **15** between tap **14** and ground, reference or common terminal **16** and a second portion **17** between tap **14** and the transistor collector. The base of transistor Q1 is effectively connected to ground terminal **16**. The winding polarities are indicated by the dots.

Referring to FIG. **2**, transistor Q1 is represented as an ideal common base circuit having an input admittance y_{11} between base and emitter that is infinite, and output admittance y_{22} between collector and ground that is zero, a reverse transfer admittance y_{12} that is zero and a ratio of forward transfer admittance y_{21} to input admittance y_{11} that is unity.

Referring to FIG. **3**, there is shown an ideal equivalent circuit of the amplifier with a source resistance R_s connected between input terminal 11 and ground **16**, a load resistance R_L connected between output terminal 12 and ground **16**, and transistor Q1 represented as an ideal current source **21** connected between ground **16** and node d delivering the same current i_a into node *d* that enters node a and produces a potential v_a across primary winding **13**. Voltages across portions **17** and **15** and the currents flowing in the various leads are as indicated in FIG. **3**.

The following relationships hold:

$$v_m = nv_a \tag{1}$$

$$v_m = mv_a \tag{2}$$

$$i_a + ni_a = mi_m \tag{3}$$

Since a flows through both the single primary turn and the n turns, then

$$i_m = [(1+n)/m]\ i_a$$

With the transformer ideal, and the dependent current generator at node d, the following relationships hold:

$$v_b = mv_a \tag{4}$$

$$i_b = -(i_a + i_m)$$

$$i_b = -[(m + n + 1)/m]\ i_a \tag{5}$$

Hence

$$v_b i_b = -(m + n + 1)\, i_a v_a \tag{6}$$

$$v_b/i_b = -[m^2/(m+n+1)]\ v_a/i_a \tag{7}$$

With a voltage source in series with source resistance R_s, i_b flows outward into R_L, and

$$v_b/i_b = -R_L \tag{8}$$

Hence from (7)

$$v_a/i_a = [(m+n+1)/m^2]\ R_L = R_{in} \tag{9}$$

With a voltage source in series with R_L, i_a flows outward into R_s, and

$$v_a/i_a = -R_s \tag{10}$$

Hence from (7)

$$v_b/i_b = [m^2/(m+n+1)]R_s = R_{out} \tag{11}$$

The input impedance matches the source resistance R_s if m and n are related by

$$R_{in} = R_s = [(m+n+1)/m^2]R_L \tag{12}$$

If this expression for R_s is substituted in equation (11), $R_{out} = R_L$, the desirable situation of two-way impedance match. Rewriting equation (12) to relate m and n for two-way impedance match,

$$n = m^2(R_s/R_L) - m - 1 \tag{13}$$

Note that if m is an integer and R_s and R_L are related so that $m^2(R_s/R_L)$ is also an integer, then n will also be an integer.

It is assumed that equation (13) is satisfied from here on. With a voltage source, v, in series with R_s, then the available power at the input is

$$P_{av_a} = v^2/4R_s \tag{14}$$

But with equation (13) satisfied, the input is matched and

$$v_a = v/2 \text{ and } P_{av_a} = v_a i_a \tag{15}$$

The power delivered to the load at node b is

$$P_b = -v_b i_b = (m+n+1)\ P_{av_a} \tag{16}$$

The transducer gain G is the ratio of:

$$P_b/P_{av_a} = G = m+n+1 = m^2(R_s/R_L) \tag{17}$$

Likewise with the generator at node b we have

$$P_{av_b} = v^2/4R_L,\ v_b = v/2 \text{ and } v_b i_b = P_{av_b}$$

Hence:

$$P_a = -v_a i_a = [1/(m+n+1)]P_{av_b} \tag{18}$$

and the reverse gain G_r is given by

$$P_a/P_{av_b} = G_r = 1/G \tag{19}$$

With the source at node a the load impedance, R_{Lc}, presented to the collector is

$$R_{Lc} = v_a/i_a = [(n+m)\ v_a]/i_a \tag{20}$$

but $v_a/i_a = R_s$. Hence:

$$R_{Lc} = (n+m)\ R_s \tag{21}$$

Referring to FIG. 4, the equivalent circuit of FIG. 3 is redrawn to facilitate determining the source impedance presented to the emitter as seen looking in at the emitter feed point between node c and ground 16. Assuming that node c is positive with respect to ground, the voltages and currents are as indicated in FIG. 4 and the following relationships occur.

$$R_{ec} = v_c/i_a = [v_a + (v_a/m)]/i_a \tag{22}$$

$$v_a = i_a R_s;\ v_b = i_b R_L \tag{23}$$

$$i_b = [(m+n+1)/m]i_a \quad (24)$$

Hence:

$$R_{ae} = R_s + [(m+n+1)/m^2]R_L \quad (25)$$

But comparing equation (12) with equation (25) shows that

$$R_{ae} = 2R_s \quad (26)$$

In summary for two-way impedance match the following relationships occur:

Turns Ratio:	$n = m^2 (R_s/R_L) - m - 1$	(13)
Forward Gain:	$G = m^2 (R_s/R_L)$	(17)
Reverse Gain:	$G_r = 1/G$	(19)
Collector Load Impedance:	$R_{Lc} = (n+m) R_s$	(21)
Emitter Source Impedance:	$R_{se} = 2R_s$	(26)

Referring to FIG. **5**, there is shown a schematic circuit diagram of a preferred embodiment of the invention showing typical parameter values. The same reference symbols identify corresponding elements throughout the drawing. FIG. **5** includes an input coupling capacitor **22**, an output coupling capacitor **23**, an emitter biasing resistor **24** in series with an *r-f* choke **25**, biasing resistors **26** and **27**, bypass capacitors **31** and **32** and B+ terminal **33**. The circuit dissipates negligible *r-f* power. Resistors **24**, **26** and **27** do not dissipate *r-f* power because negligible *r-f* current flows through them. Were transformer **T1** and transistor **Q1** ideal and lossless, there would be essentially no *r-f* power loss between input and output. Because of the nature of the circuit, the circuit dynamic range corresponds substantially to that of transistor **Q1**.

With the circuit of FIG. **5** and **10** ma. delivered into terminal **33** at 15 volts, the invention had a gain of 8dB± 0.25 dB from 5 to 350 MHz. For input and output impedance of 50 ohms the maximum VSWR was 1.5 from 5 to 100 MHz and 2 from 100 to 250 MHz. The maximum noise figure was 1.2 dB from 5 to 150 MHz and 1.5 dB from 150 to 200 MHz. The minimum power output at 1dB compression over 5 to 150 MHz was 10 dBm and from 150 to 200 MHz **9** dBm.

There has been described a novel *r-f* amplifying circuit characterized by matching source and load impedances and good amplification over a relatively broad bandwidth while using relatively few components, components that need not be adjusted and are relatively economical. It is evident that those skilled in the art may now make numerous uses and modifications of and departures from the specific embodiments described herein without departing from the inventive concepts. Consequently, the invention is to be construed as embracing each and every novel feature and novel combination of features present in or possessed by the apparatus and techniques herein disclosed and limited solely by the spirit and scope of the appended claims.

What is claimed is:

1. Amplifying apparatus comprising,
amplifying means having at least control, input and output electrodes,
a common terminal,
transformer means having at least a primary and a secondary winding,
said secondary winding having a tap intermediate to first and second portions thereof,
an input terminal,
an output terminal,
means for coupling said output terminal to said tap,
means for coupling said primary winding between said input terminal and said input electrode,
said first portion being coupled between said tap and said common terminal,
said second portion being coupled between said tap and said output electrode,
and means for coupling said control electrode to said common terminal.

2. Amplifying apparatus in accordance with claim **1** wherein the turns ratio between said first portion and said primary winding is m and between said second portion and said primary winding is n with $n = m^2 R_s/R_L - m - 1$ wherein R_s is a predetermined source resistance and R_L is a predetermined load resistance.

3. Amplifying apparatus in accordance with claim **2** and further comprising said source resistance coupled between said input terminal and said common terminal and said load resistance coupled between said output terminal and said common terminal.

4. Amplifying apparatus in accordance with claim **1** wherein said amplifying means comprises a transistor and said control, input and output electrodes comprise base, emitter and collector electrodes, respectively.

5. Amplifying apparatus in accordance with claim **4** and further comprising,
a source of d-c operating potential connected to said collector electrode through said secondary winding,
and means for biasing said base and emitter electrodes.

6. Amplifying apparatus in accordance with claim **5** wherein the means for biasing said base electrode comprises a first resistor connected between said source of d-c potential and said base electrode and a second resistor connected between said base electrode and said common terminal and the means for coupling said base electrode to said common terminal comprises an *r-f* bypass capacitor and further comprising,
another *r-f* bypass capacitor coupling said source of a d-c potential to said common terminal.

7. Amplifying apparatus in accordance with claim **6** wherein said means for biasing said emitter electrode comprises an emitter biasing resistor in series with an *r-f* choke between said common terminal and said primary winding.

8. Amplifying apparatus in accordance with claim **7** wherein said means for coupling said primary winding between said input terminal and said emitter electrode comprises a capacitor and said means for coupling said output terminal to said tap comprises a capacitor.

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